MOSFET
(Metal Oxide Semiconductor Field Effect Transitor)

Elektronika
(TKE 4012)

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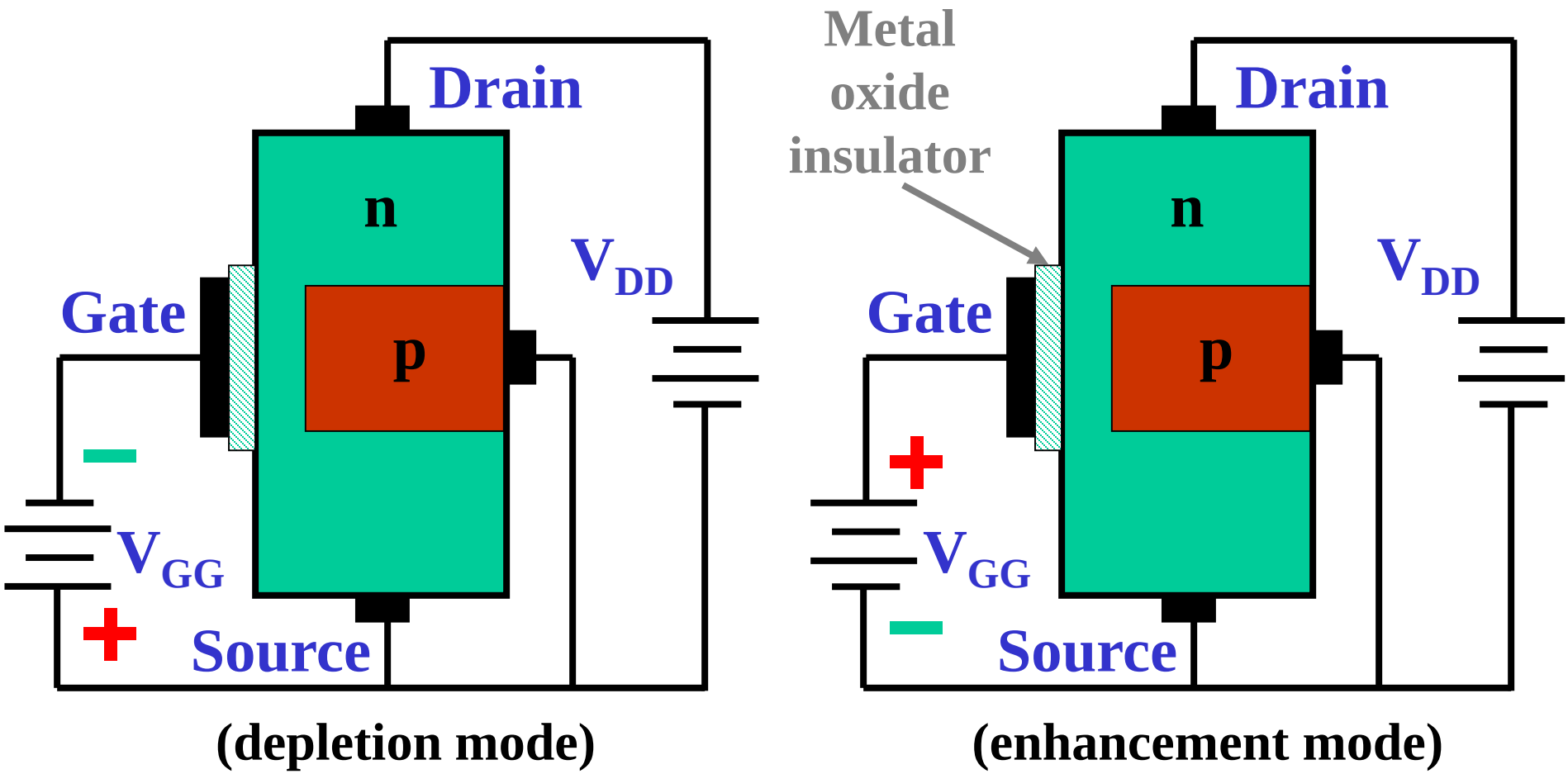
Depletion-mode MOSFET



(depletion mode)

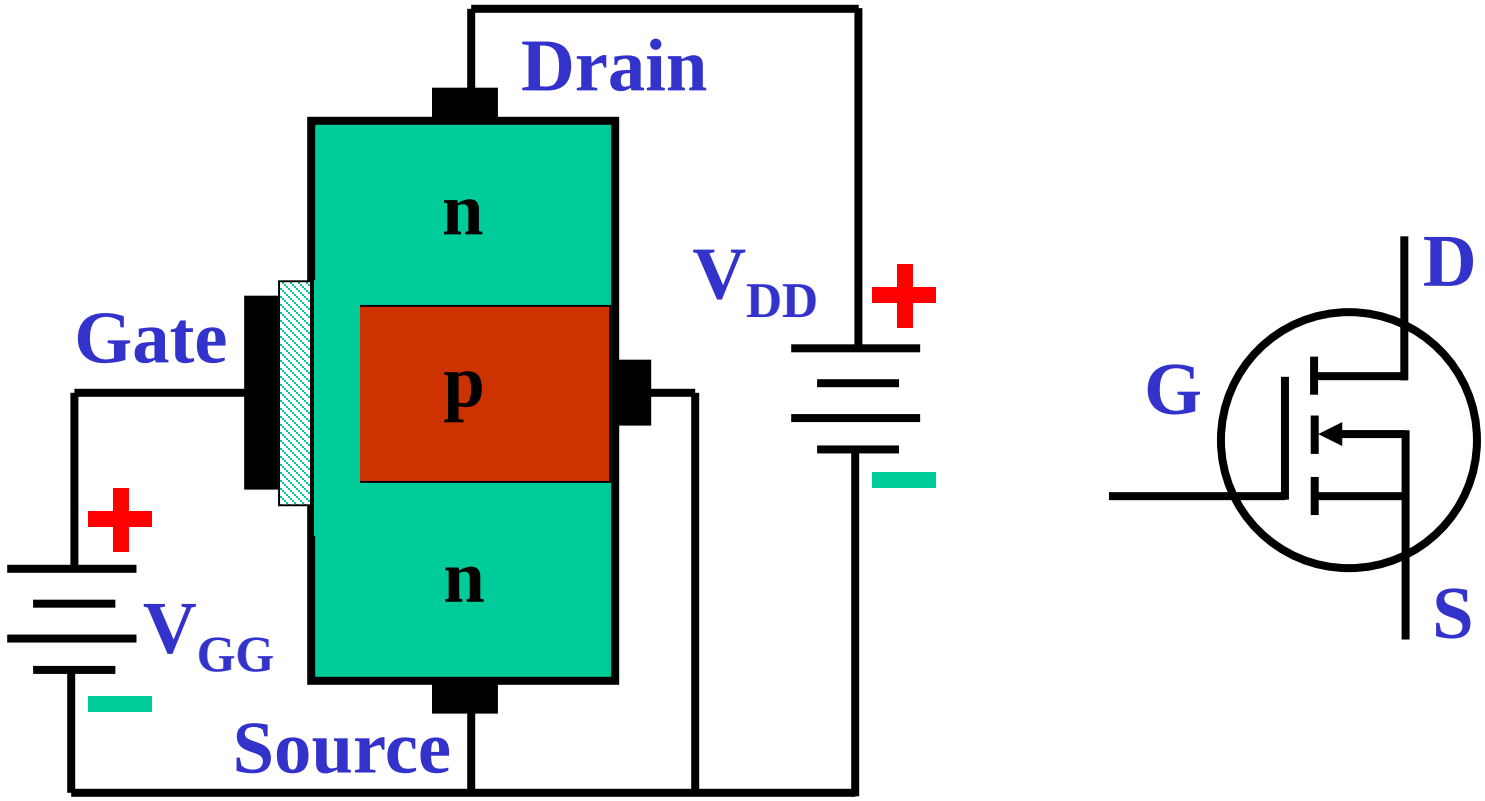
(enhancement mode)

Since the gate is insulated, this device can also be operated in the *enhancement mode*.

MOSFETs

- **Current flows through a narrow channel between the gate and substrate.**
- **SiO_2 insulates the gate from the channel.**
- ***Depletion mode* forces the carriers from the channel.**
- ***Enhancement mode* attracts carriers into the channel.**
- **E-MOSFETs are normally-off devices.**

n-channel E-MOSFET

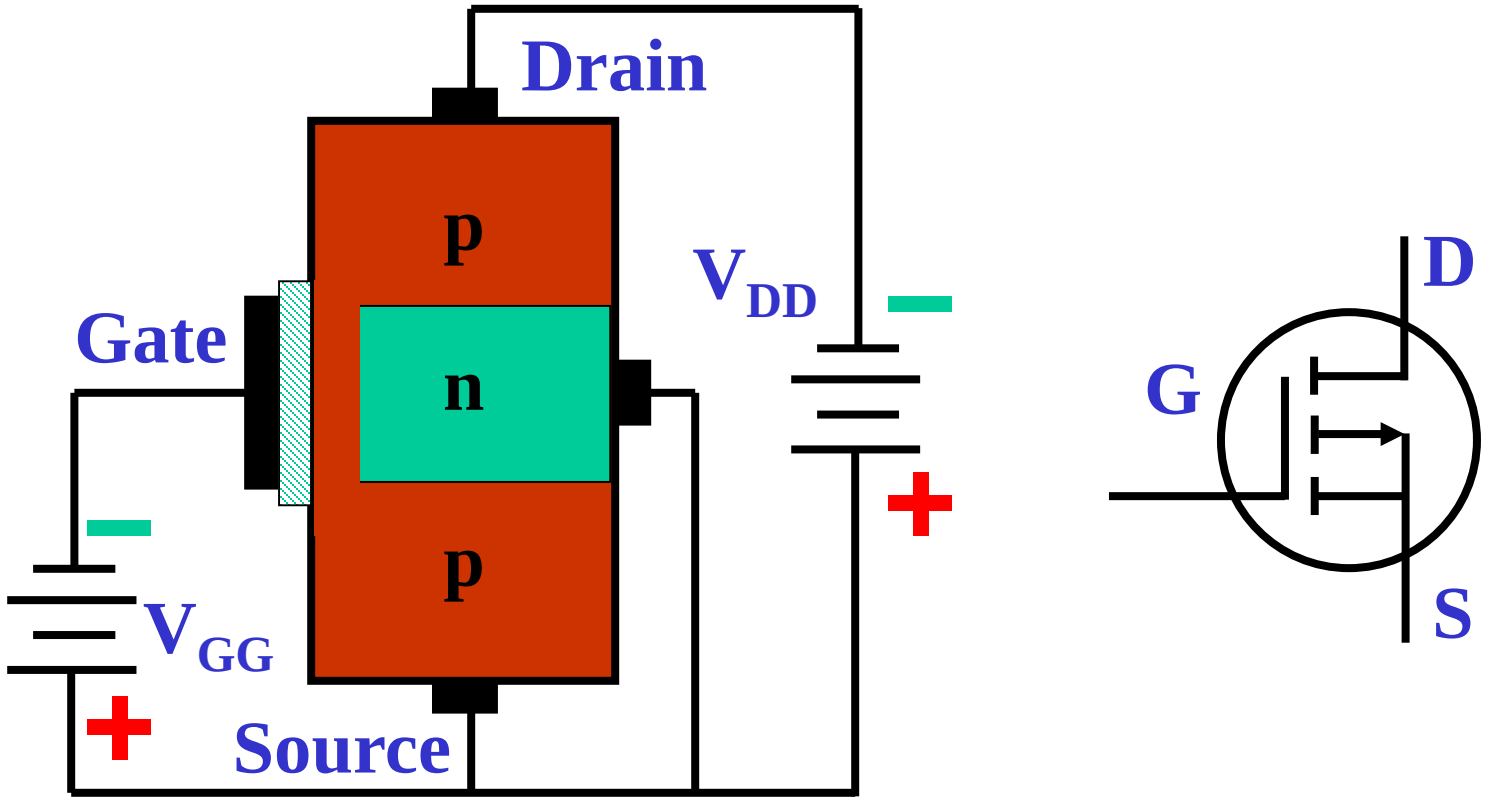


Gate bias enhances the channel and turns the device on.

n-channel E-MOSFET

- **The p-substrate extends all the way to the silicon dioxide.**
- **No n-channel exists between the source and drain.**
- **This transistor is *normally off* when the gate voltage is zero.**
- **A positive gate voltage attracts electrons into the p-region to create an n-type inversion layer and turns the device on.**

p-channel E-MOSFET

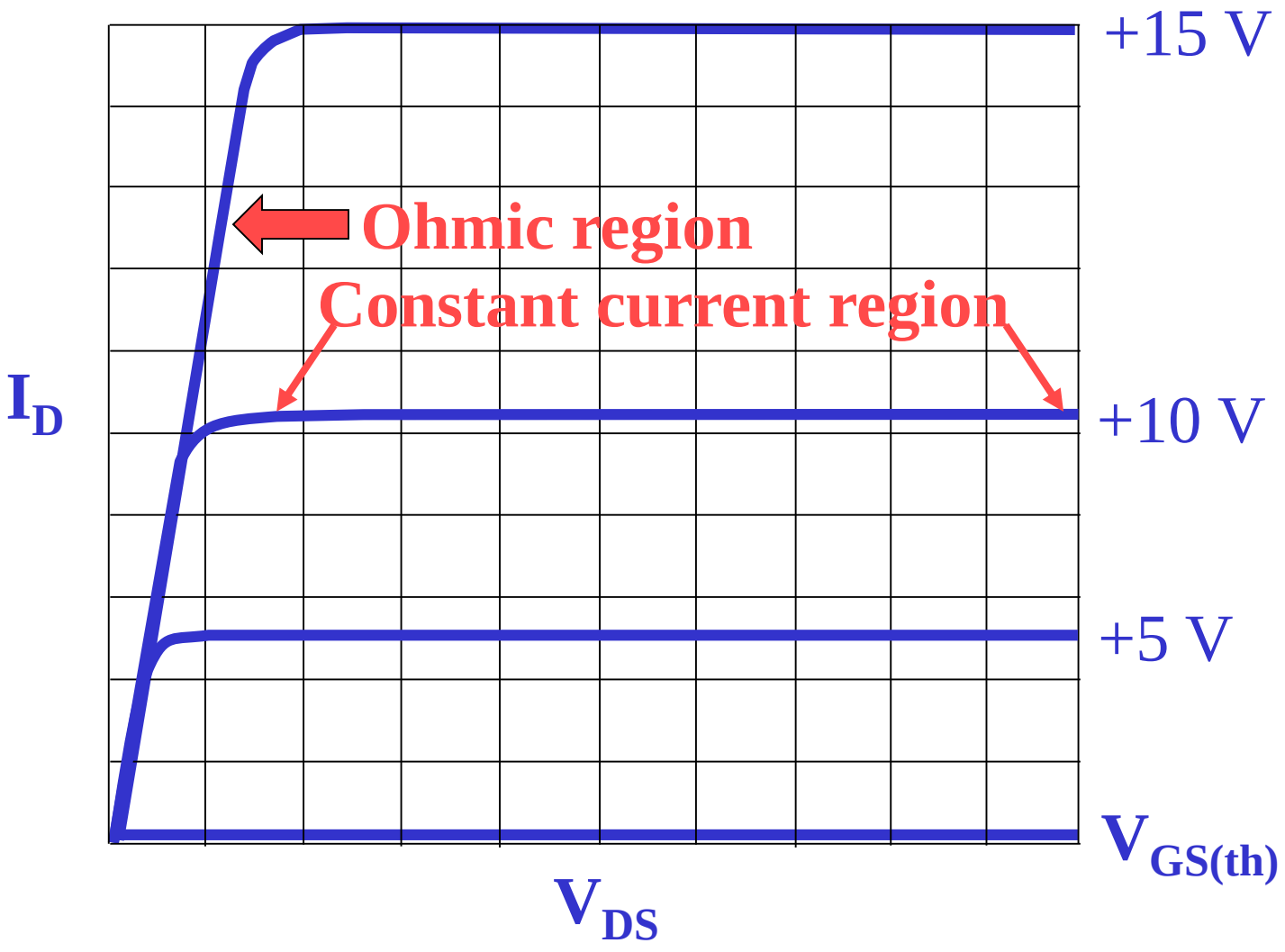


Gate bias enhances the channel and turns the device on.

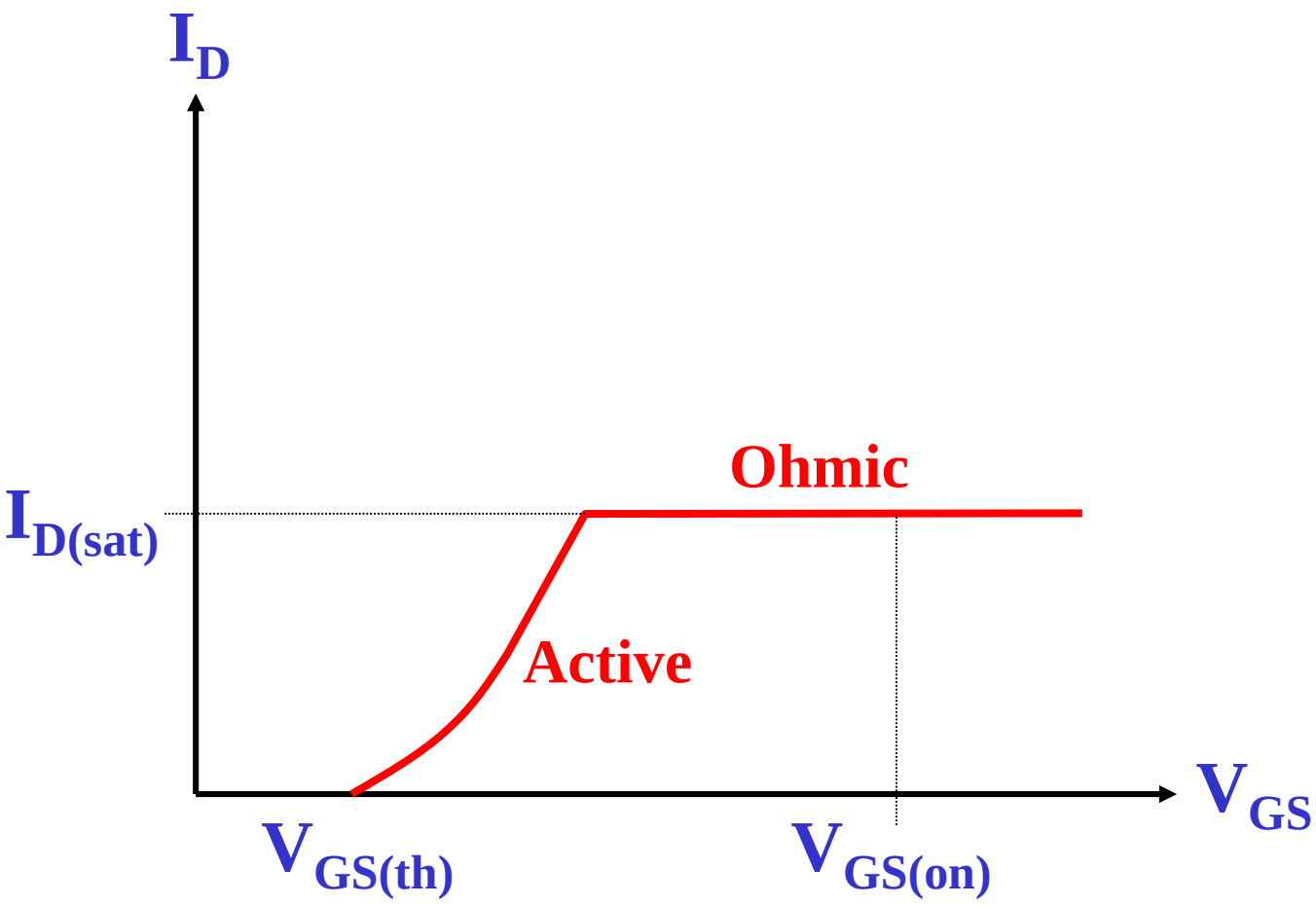
p-channel E-MOSFET

- **The n-substrate extends all the way to the silicon dioxide.**
- **No p-channel exists between the source and drain.**
- **This transistor is *normally off* when the gate voltage is zero.**
- **A negative gate voltage attracts holes into the n-region to create an p-type inversion layer and turns the device on.**

n-channel E-MOSFET drain curves



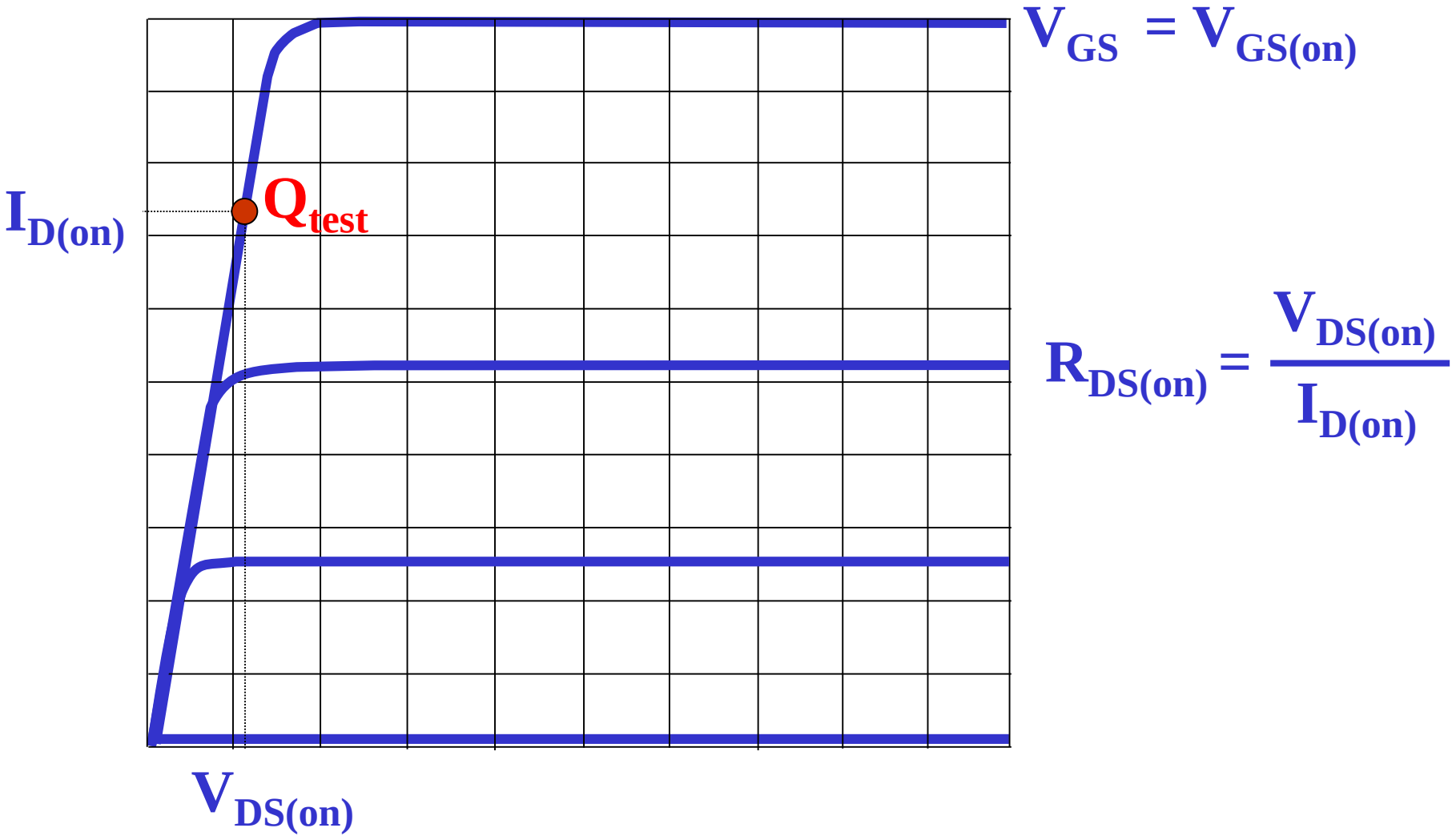
n-channel E-MOSFET transconductance curve



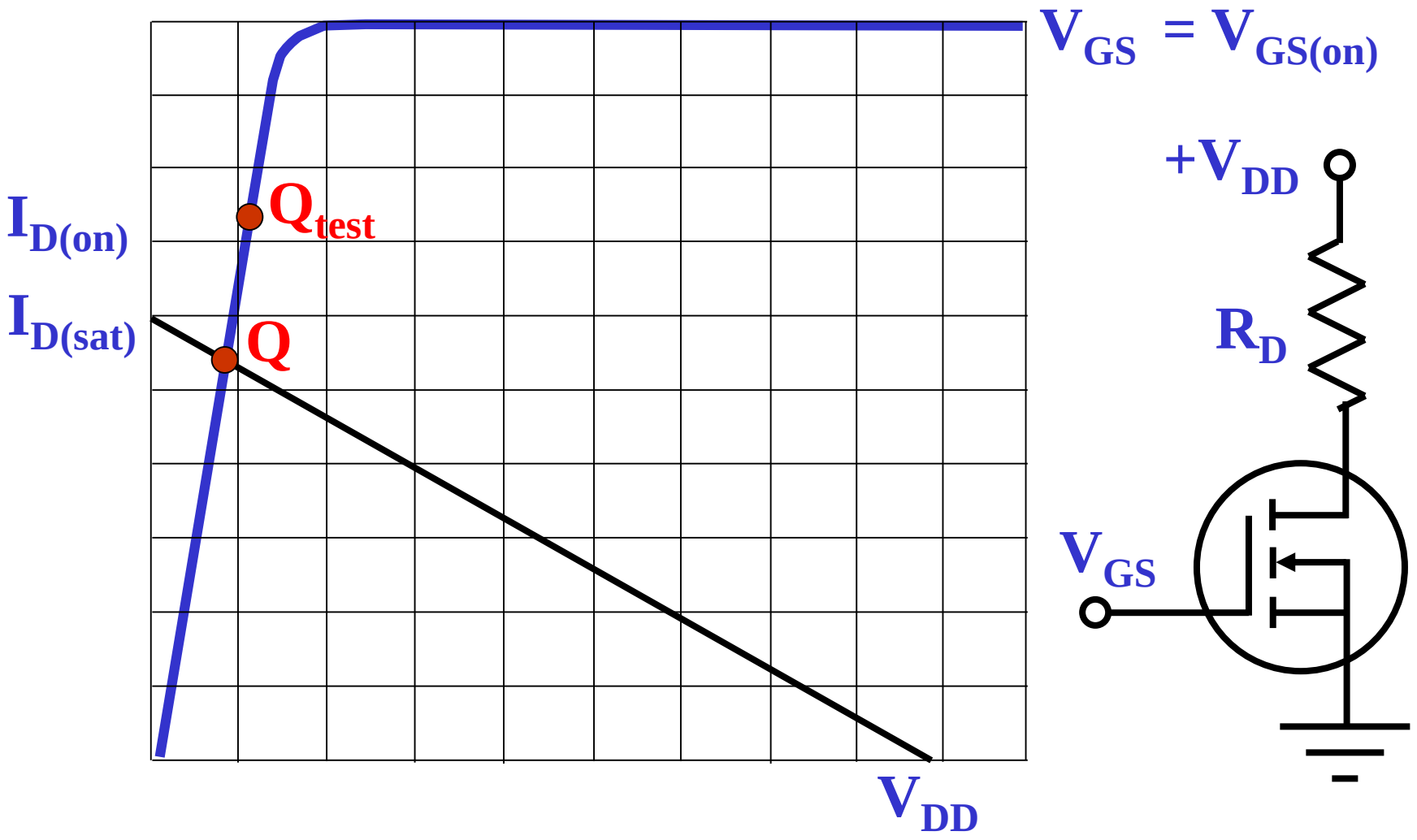
Gate breakdown

- The SiO_2 insulating layer is very thin.
- It is easily destroyed by excessive gate-source voltage.
- $V_{GS(max)}$ ratings are typically in tens of volts.
- Circuit transients and static discharges can cause damage.
- Some devices have built-in gate protection.

Drain-source on resistance

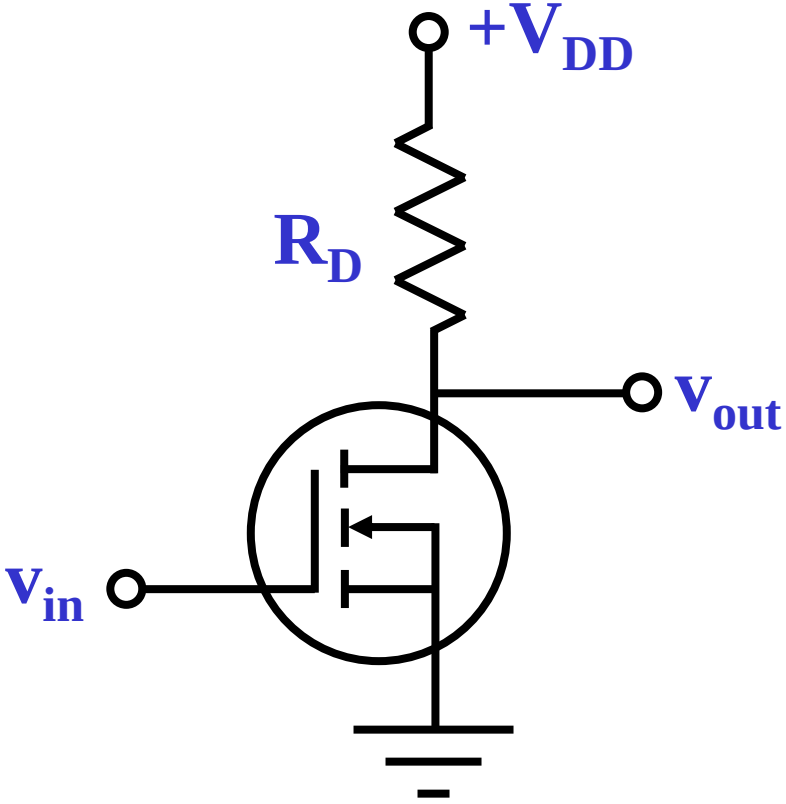


Biasing in the ohmic region

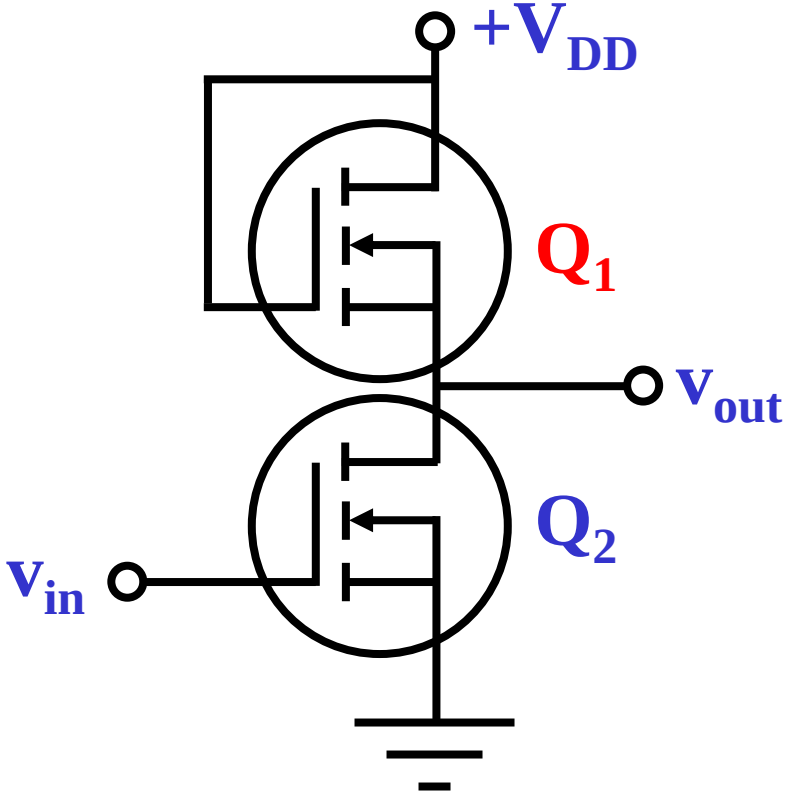


$I_{D(sat)} < I_{D(on)}$ when $V_{GS} = V_{GS(on)}$ ensures saturation

Passive and active loads



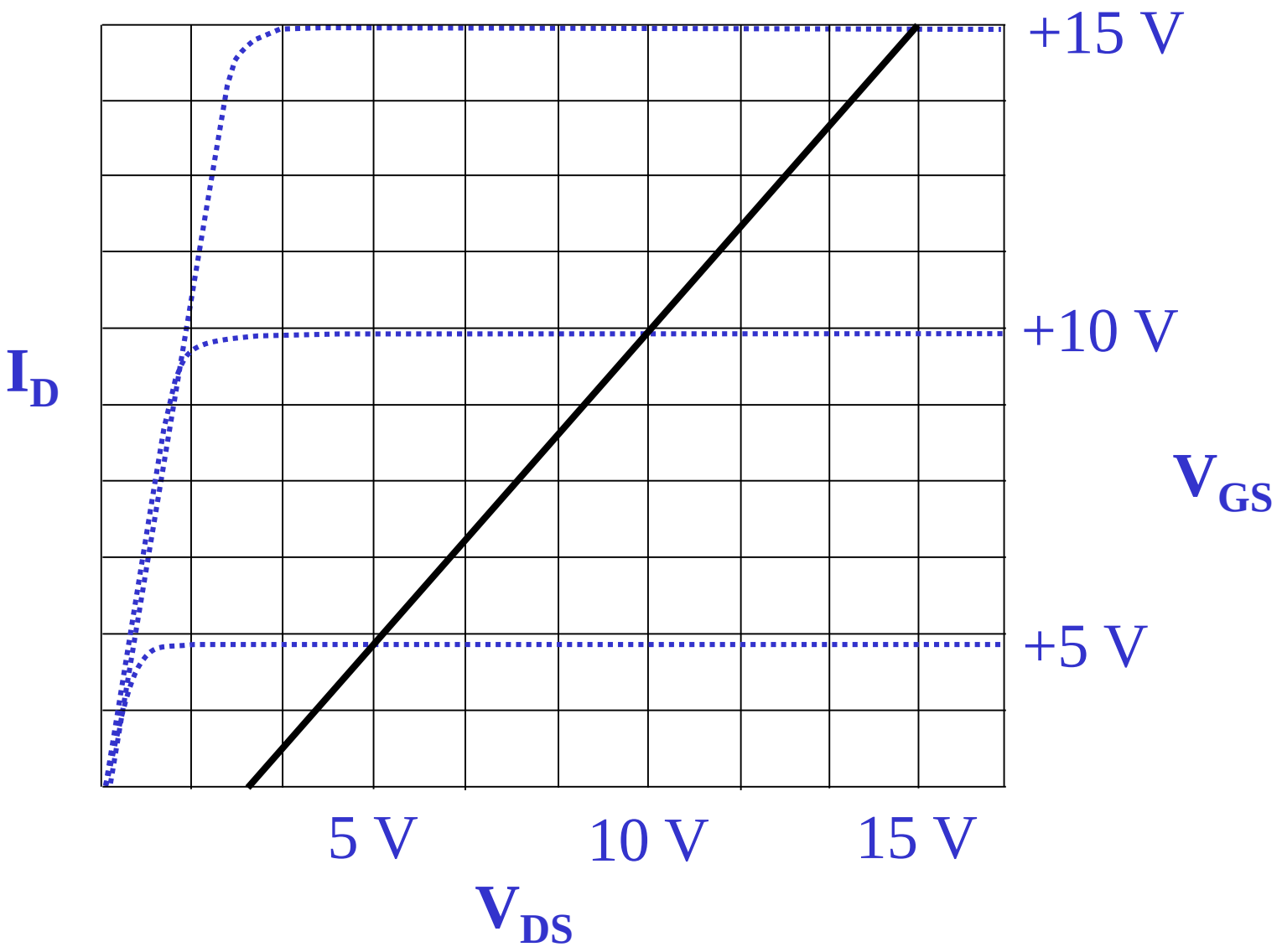
Passive load



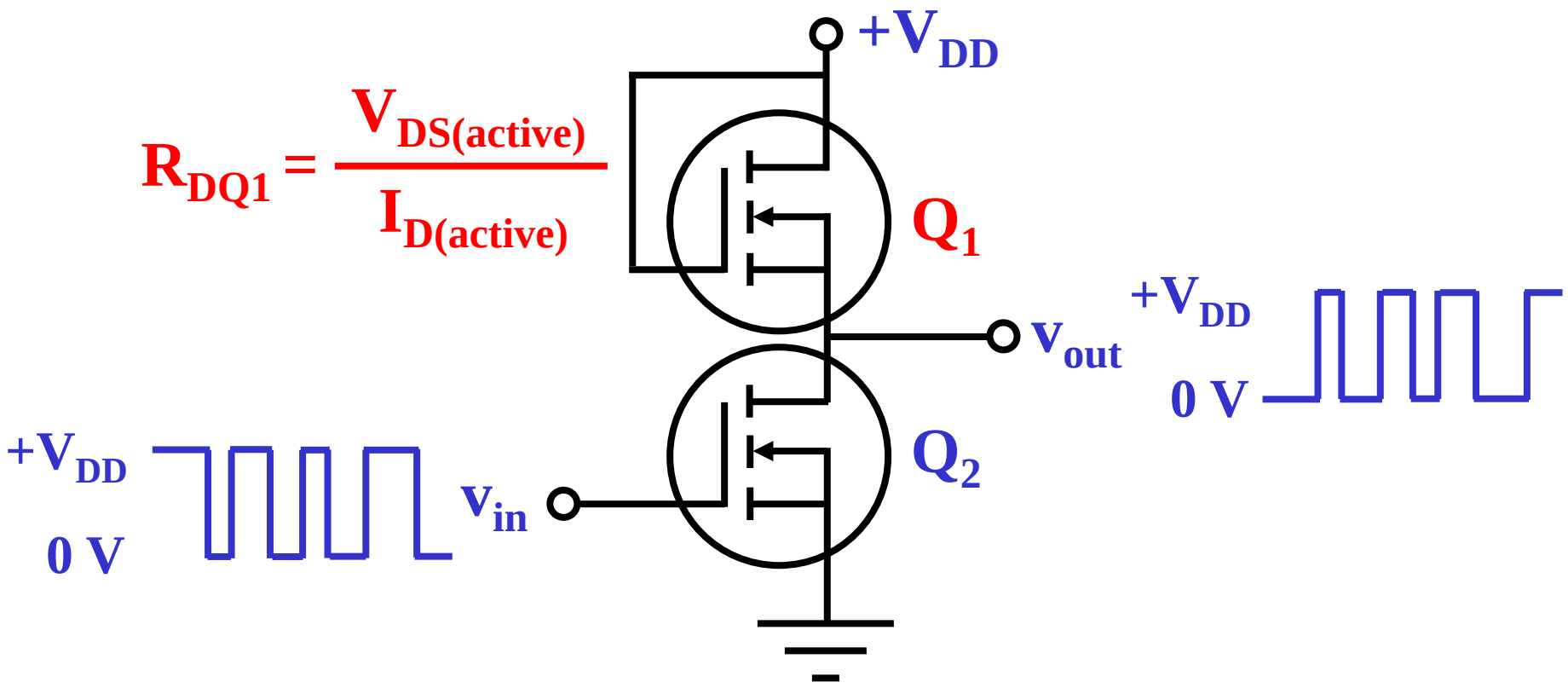
Active load

(for Q1, $V_{GS} = V_{DS}$)

$V_{GS} = V_{DS}$ produces a two-terminal curve



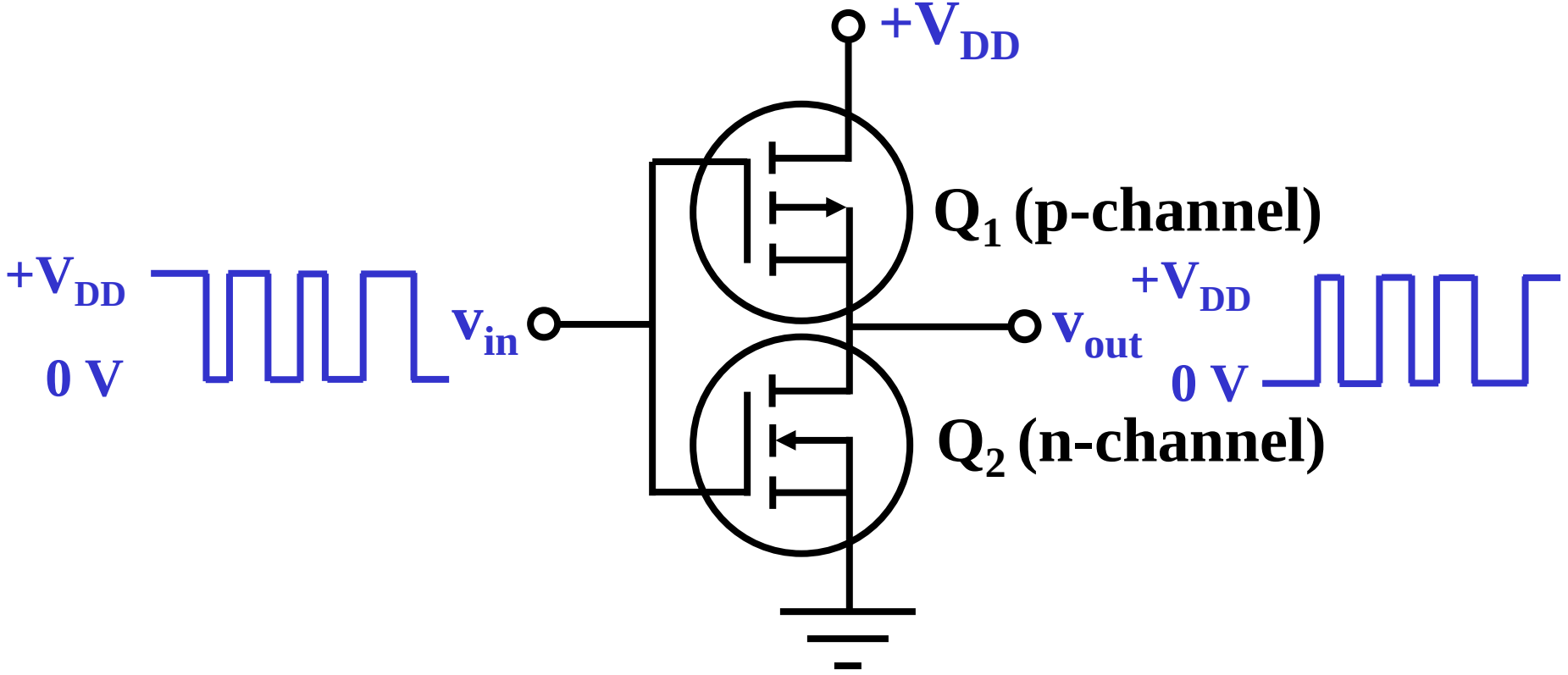
Active loading in a digital inverter



It's desirable that $R_{DSQ2(on)} << R_{DQ1}$.

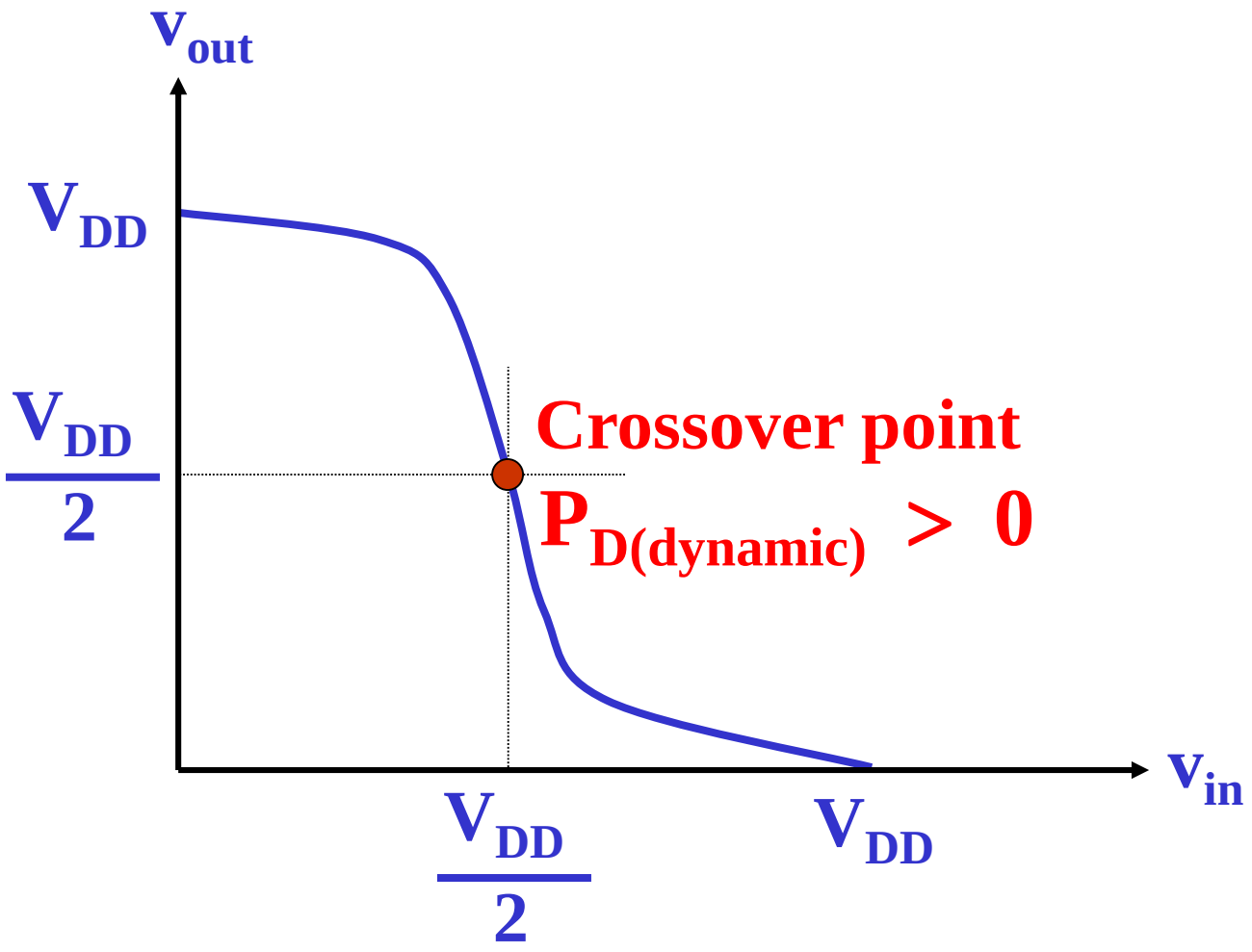
(The ideal output swings from 0 volts to +V_{DD}.)

Complementary MOS (CMOS) inverter



$P_{D(static)} \cong 0$

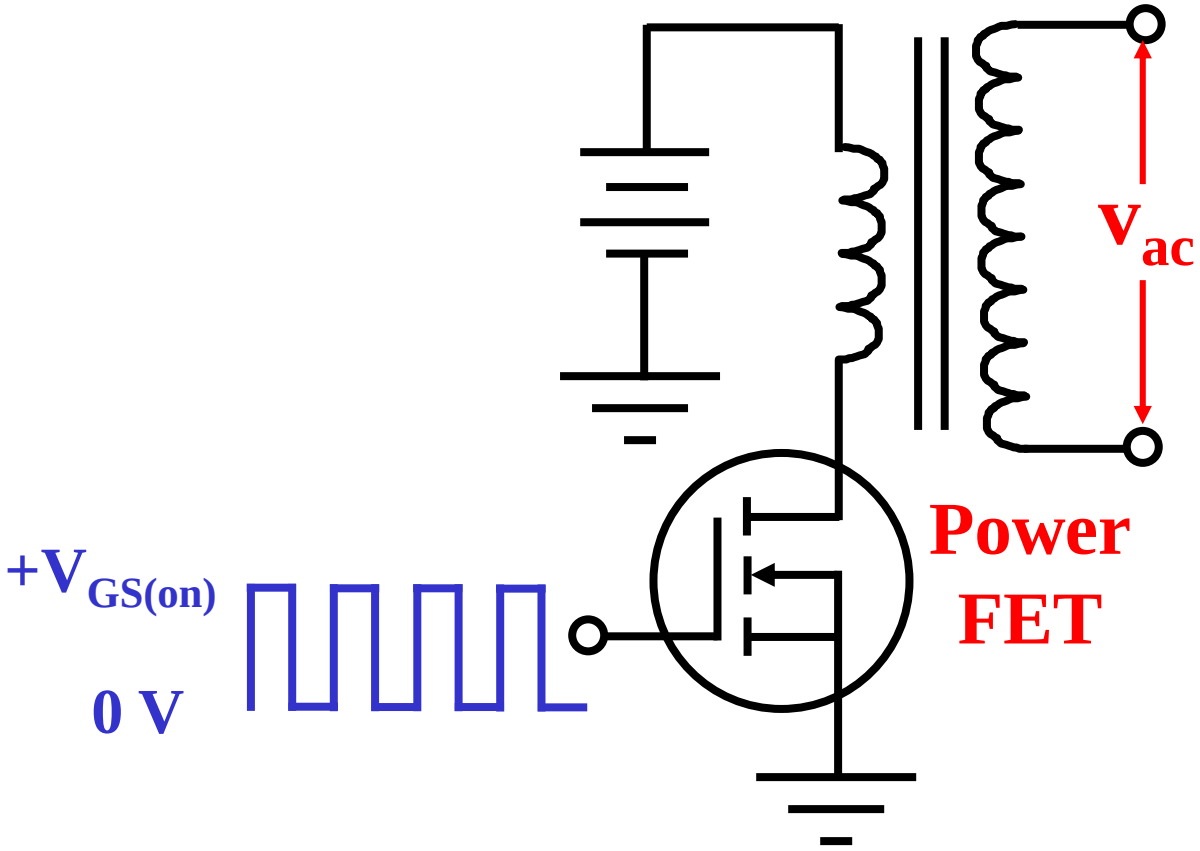
CMOS inverter input-output graph



High-power EMOS

- Use different channel geometries to extend ratings
- Brand names such as VMOS, TMOS and hexFET
- No thermal runaway
- Can operate in parallel without current hogging
- Faster switching due to no minority carriers

dc-to-ac converter



dc-to-dc converter