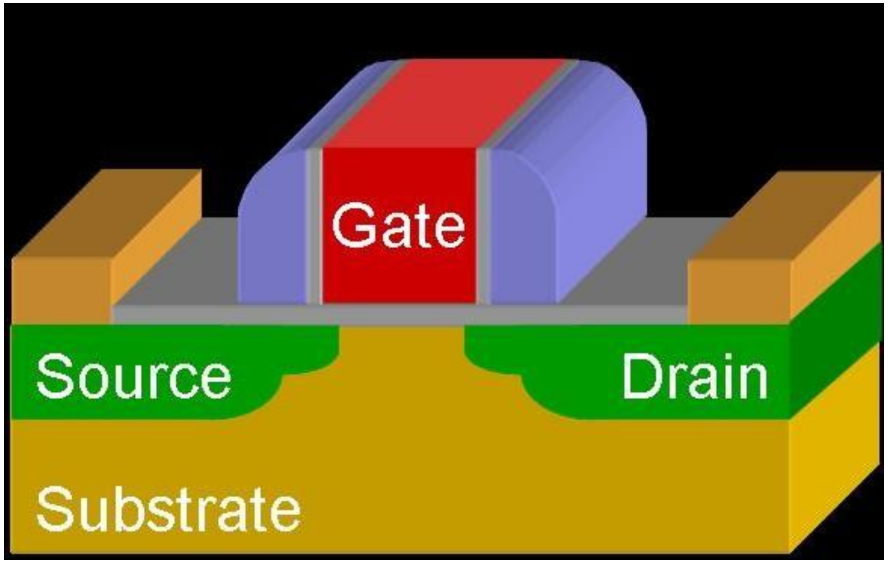
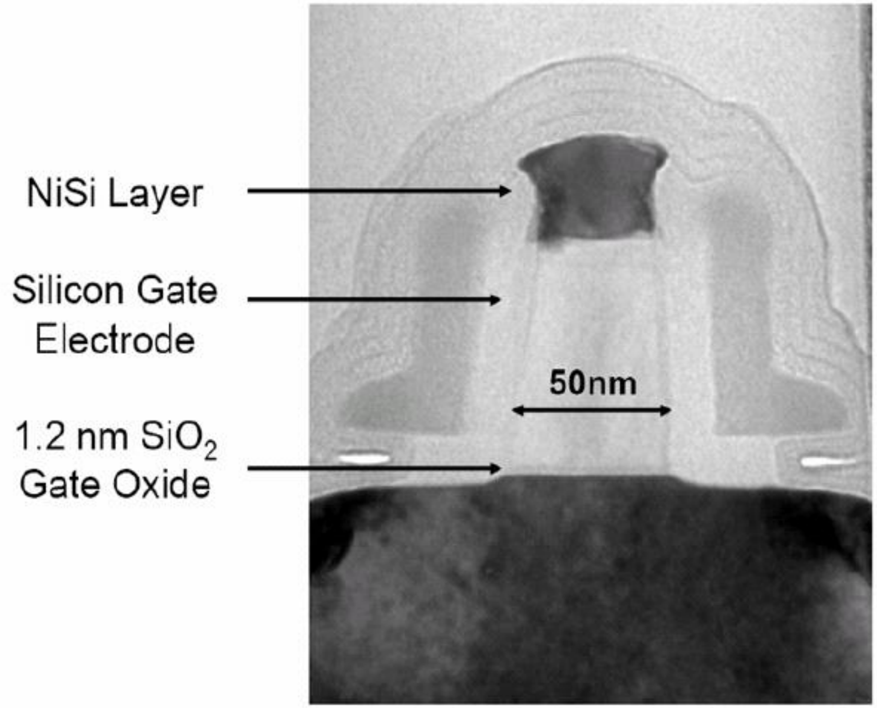
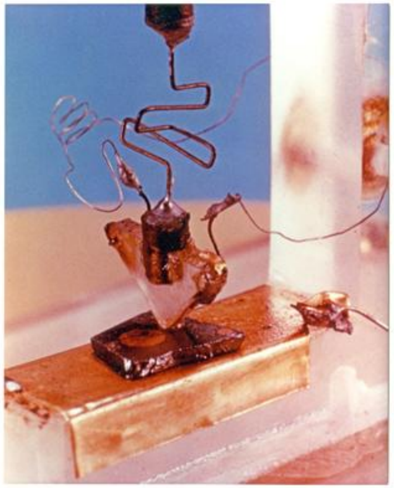
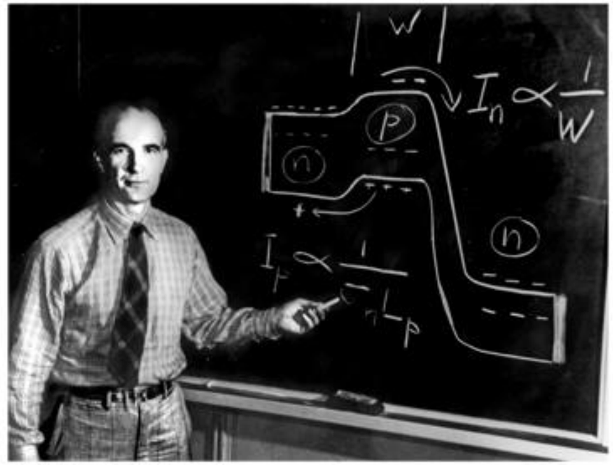
MOSFETs

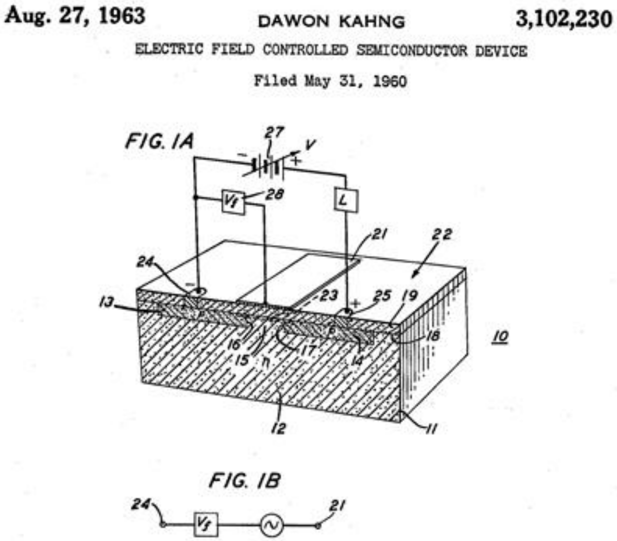

Gate
Source
Drain
Substrate


NiSi Layer
Silicon Gate Electrode
50nm
1.2 nm SiO_2 Gate Oxide

A little bit of history..

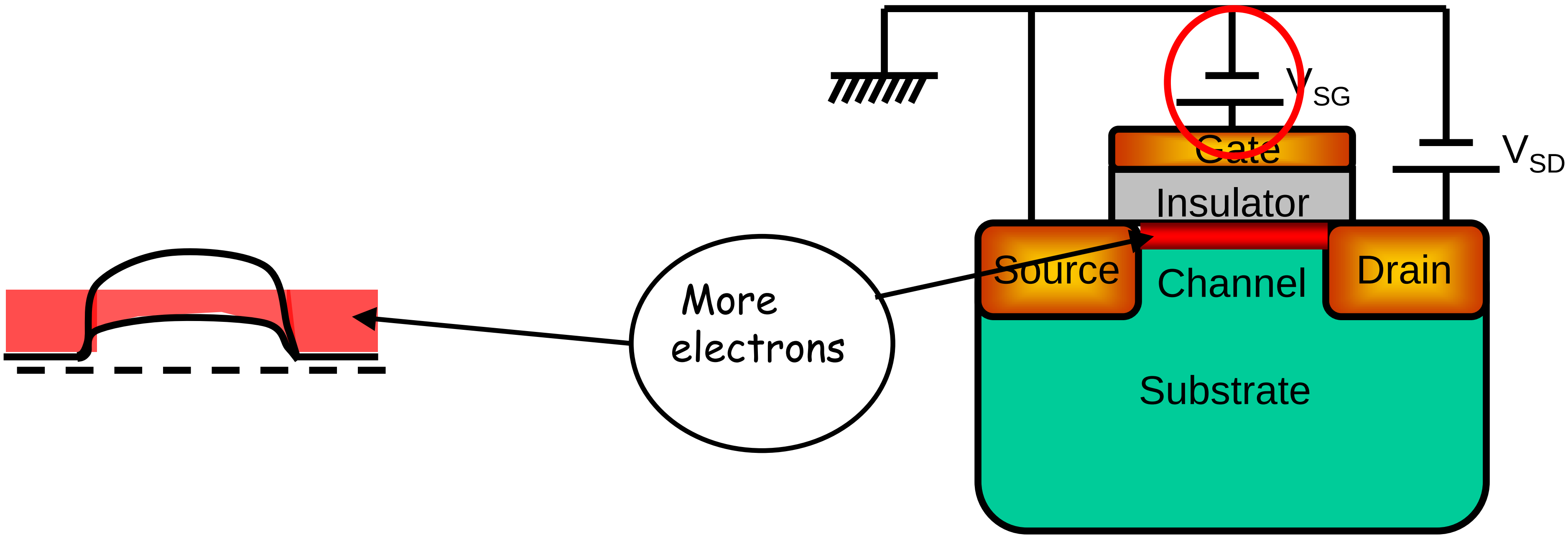






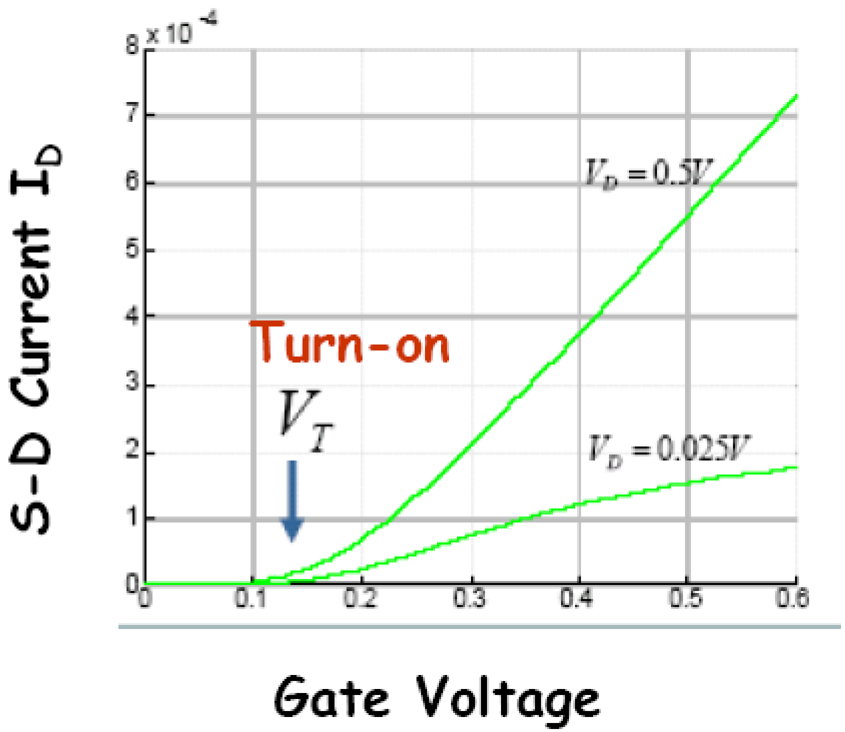
Operation of a transistor

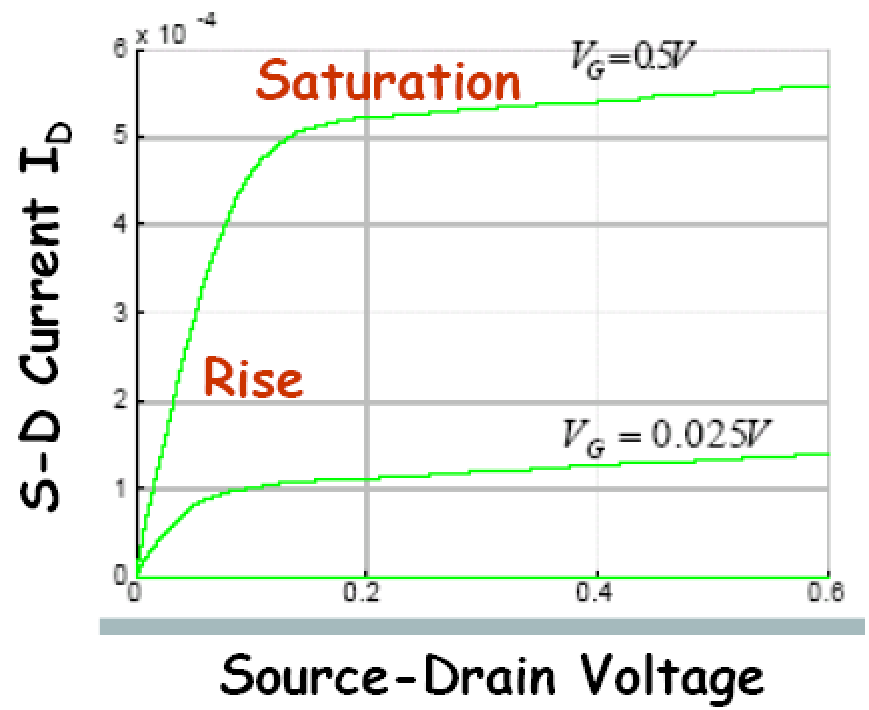
$V_{SG} > 0$
n type operation



Positive gate bias attracts electrons into channel
Channel now becomes more conductive

Operation of a transistor

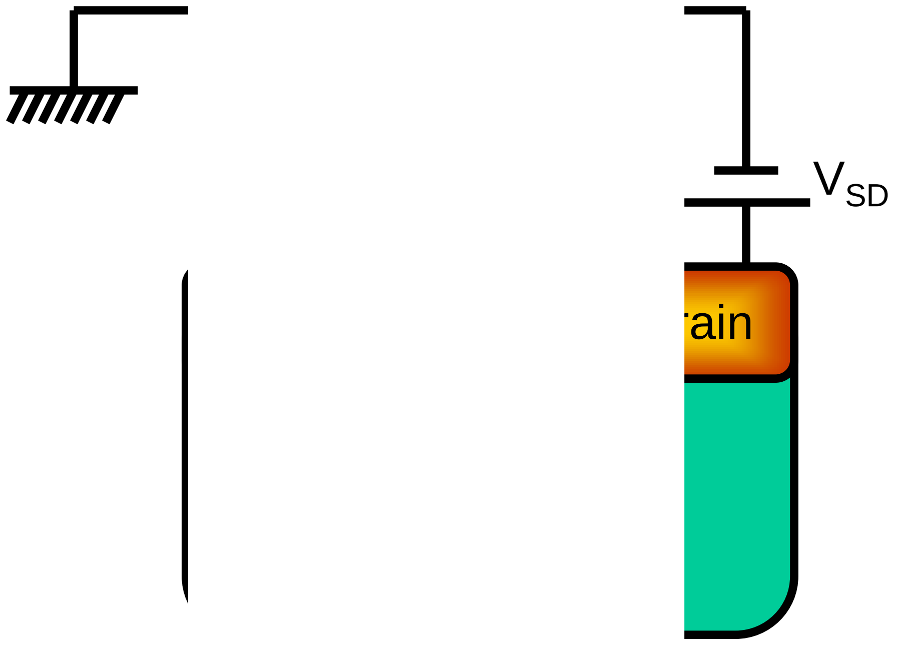




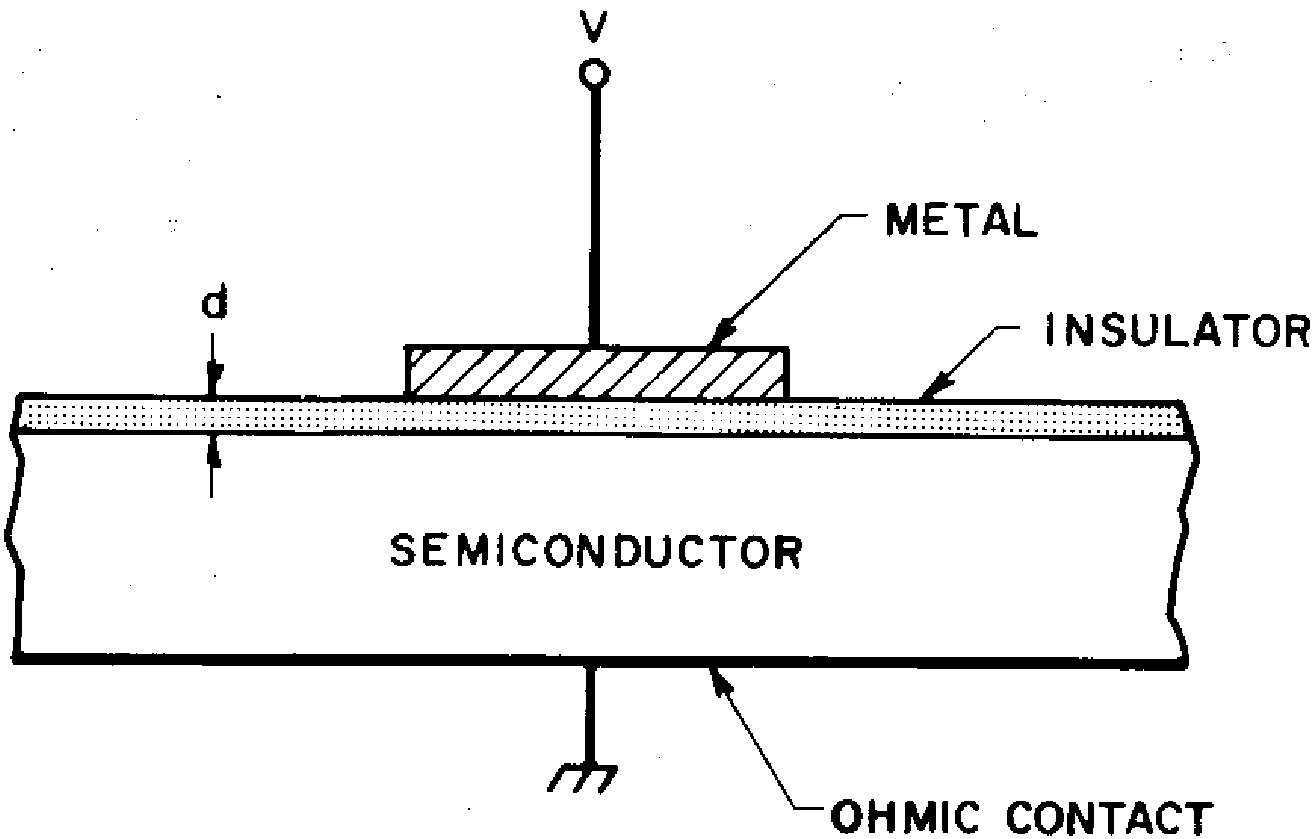
.D

Transistor turns on at high gate voltage
Transistor current saturates at high drain bias

Start with a MOS capacitor



MIS Diode (MOS capacitor) - Ideal



Questions

✓ What is the MOS capacitance? $Q_S(\psi_S)$

What are the local conditions during inversion? $\psi_{S,cr}$

How does the potential vary with position? $\psi(x)$

How much inversion charge is generated at the surface? $Q_{inv}(x,\psi_S)$

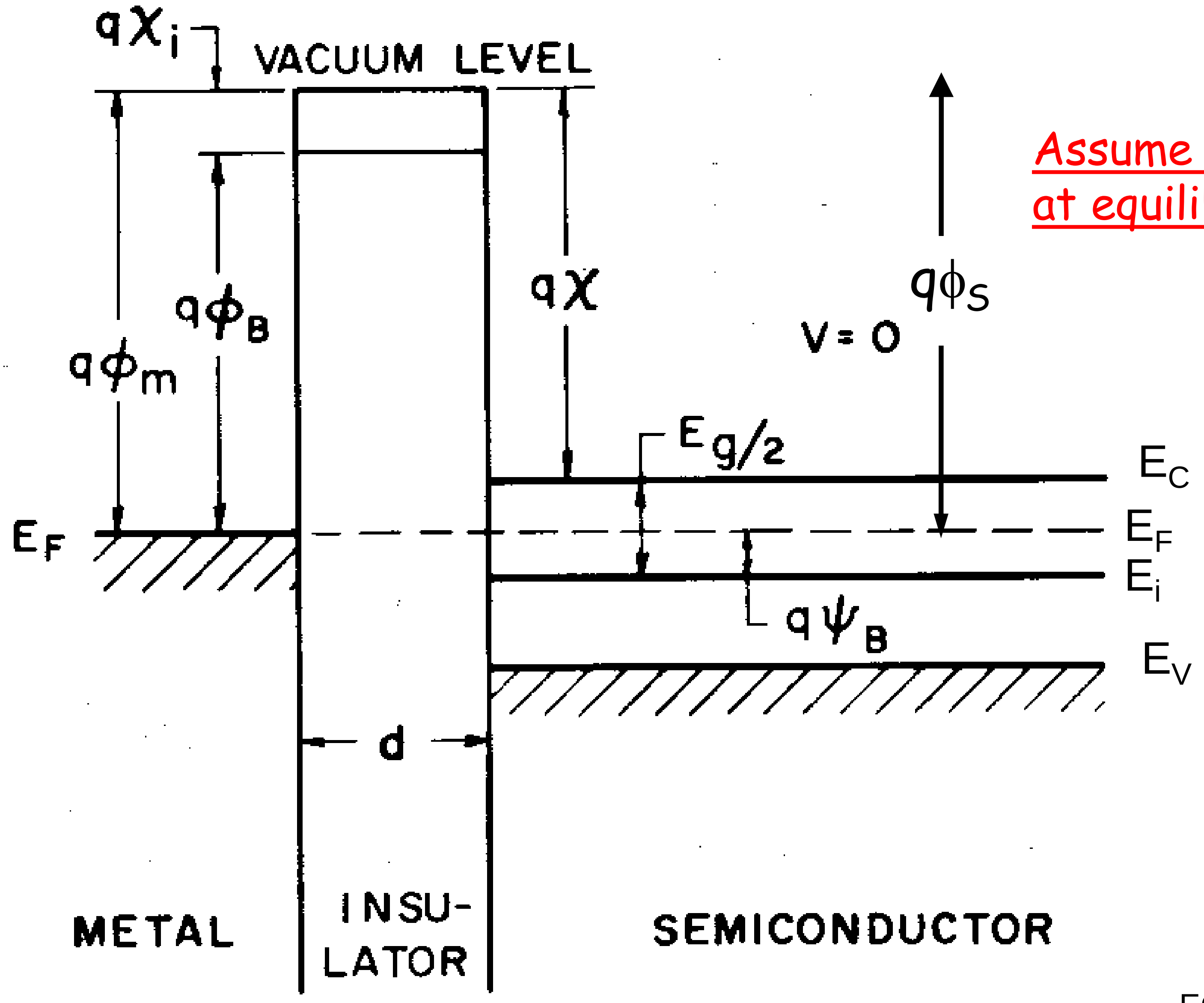
Add in the oxide: how does the voltage divide? $\psi_S(V_G)$, $\psi_{ox}(V_G)$

How much gate voltage do you need to invert the channel? V_{TH}

How much inversion charge is generated by the gate? $Q_{inv}(V_G)$

What's the overall C-V of the MOSFET? $Q_S(V_G)$

Ideal MIS Diode n-type, $V_{appl}=0$

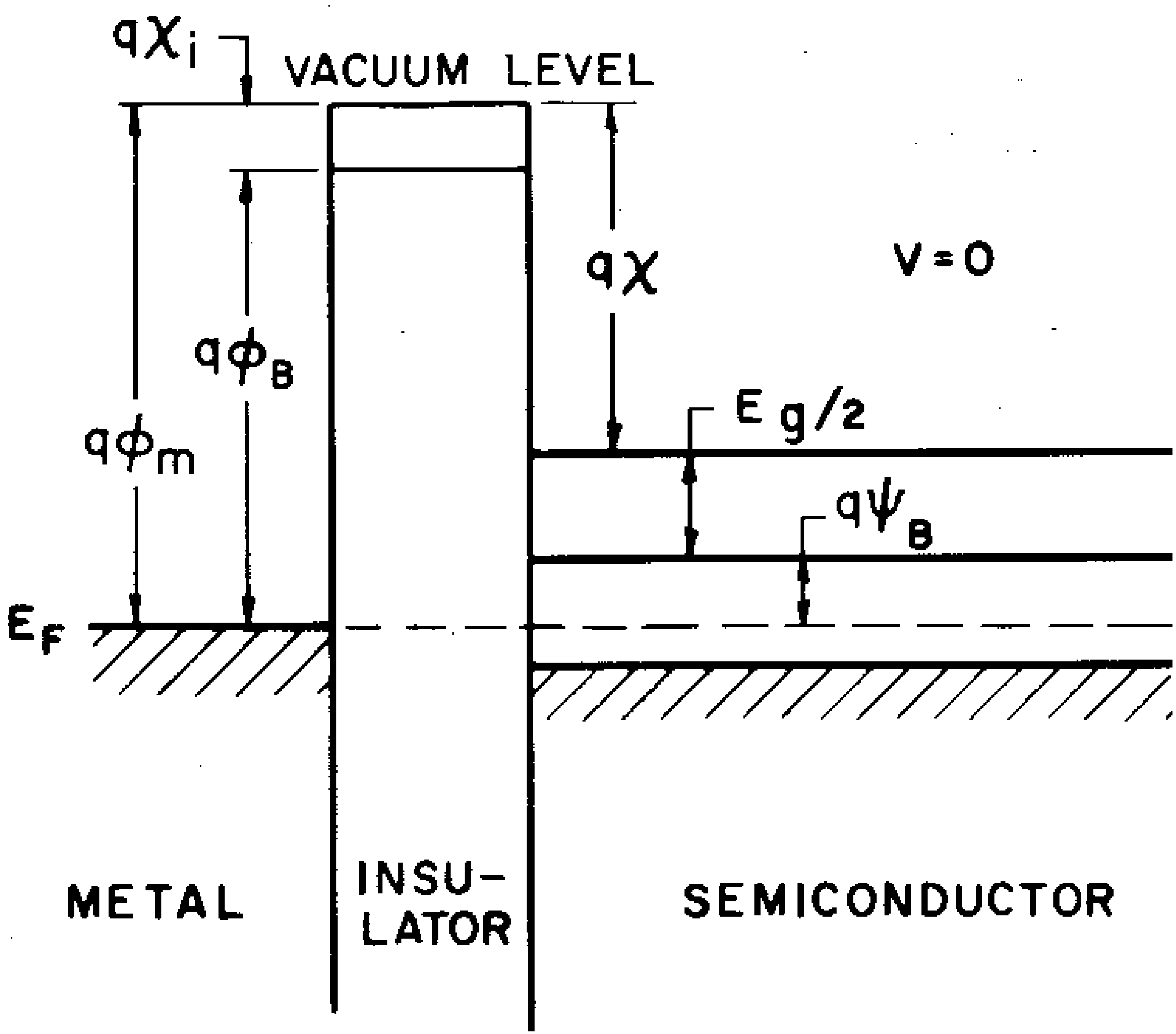


Assume Flat-band at equilibrium

Ideal MIS Diode n-type, $V_{appl}=0$

$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B \right) = 0$$

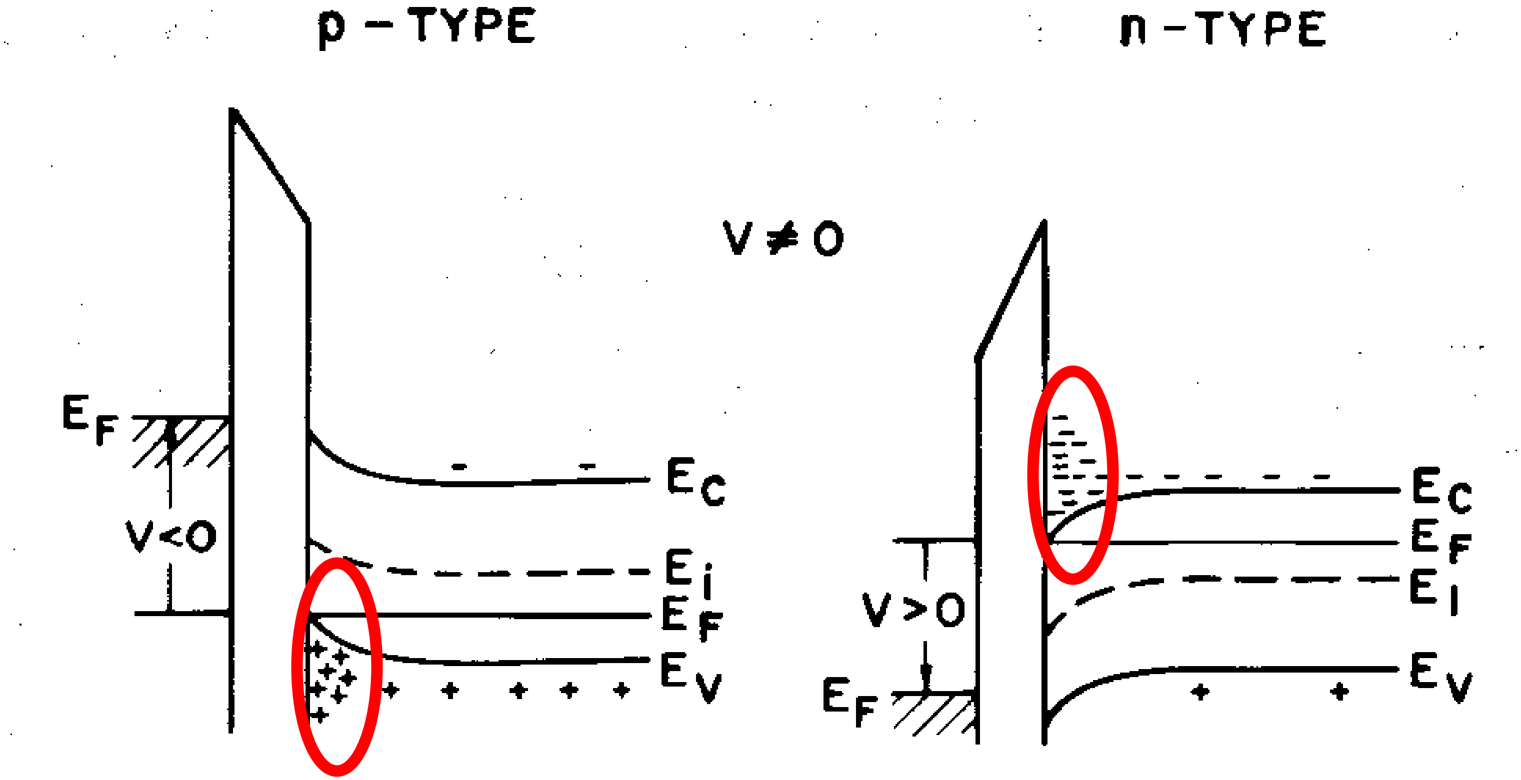
Ideal MIS Diode p-type, V_{appl}=0



Ideal MIS Diode p-type, V_{appl}=0

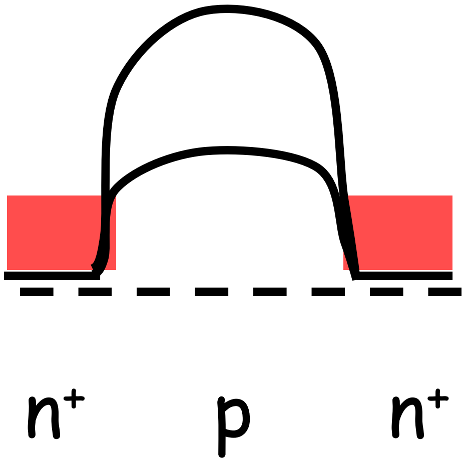
$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_B \right) = 0$$

Accumulation

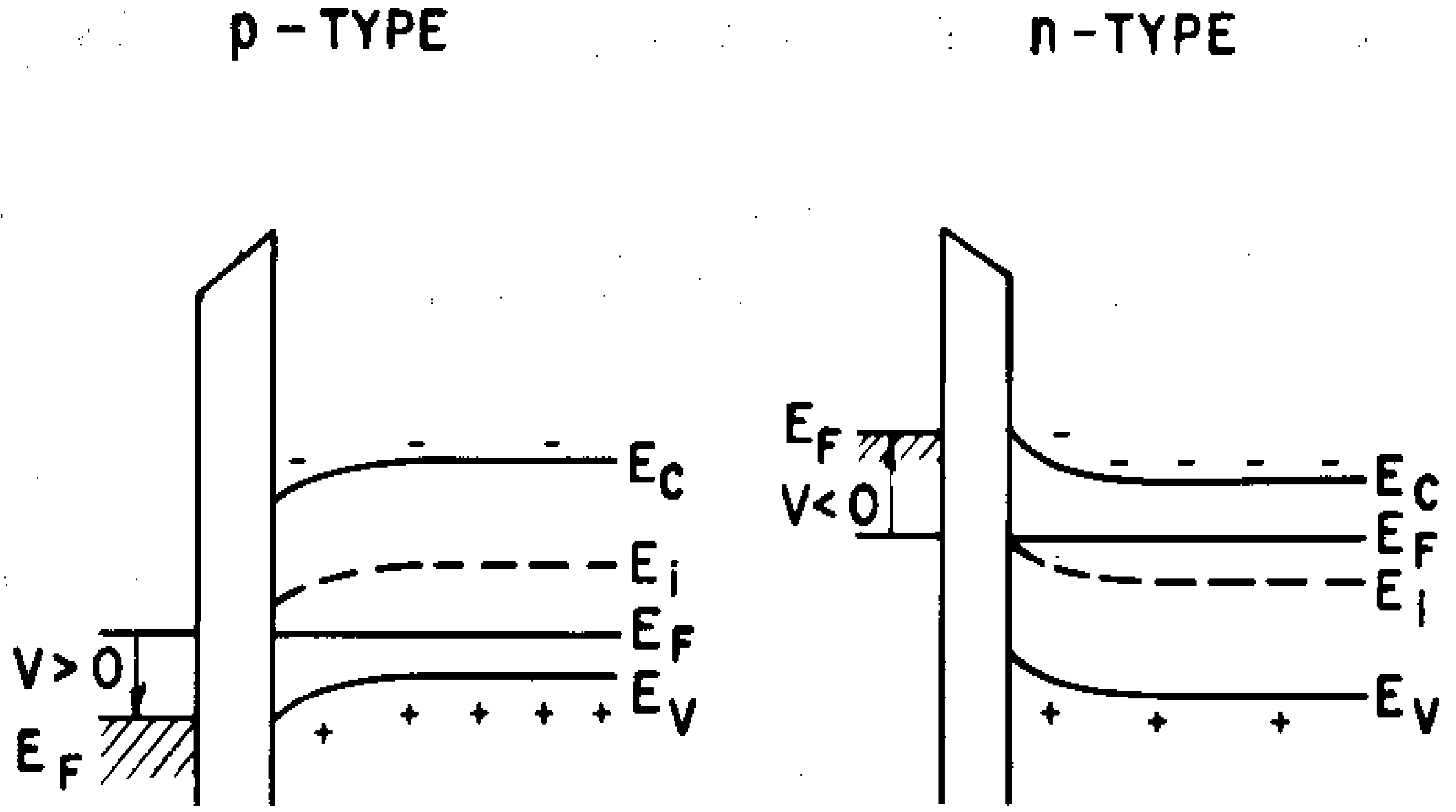


Pulling in majority carriers at surface

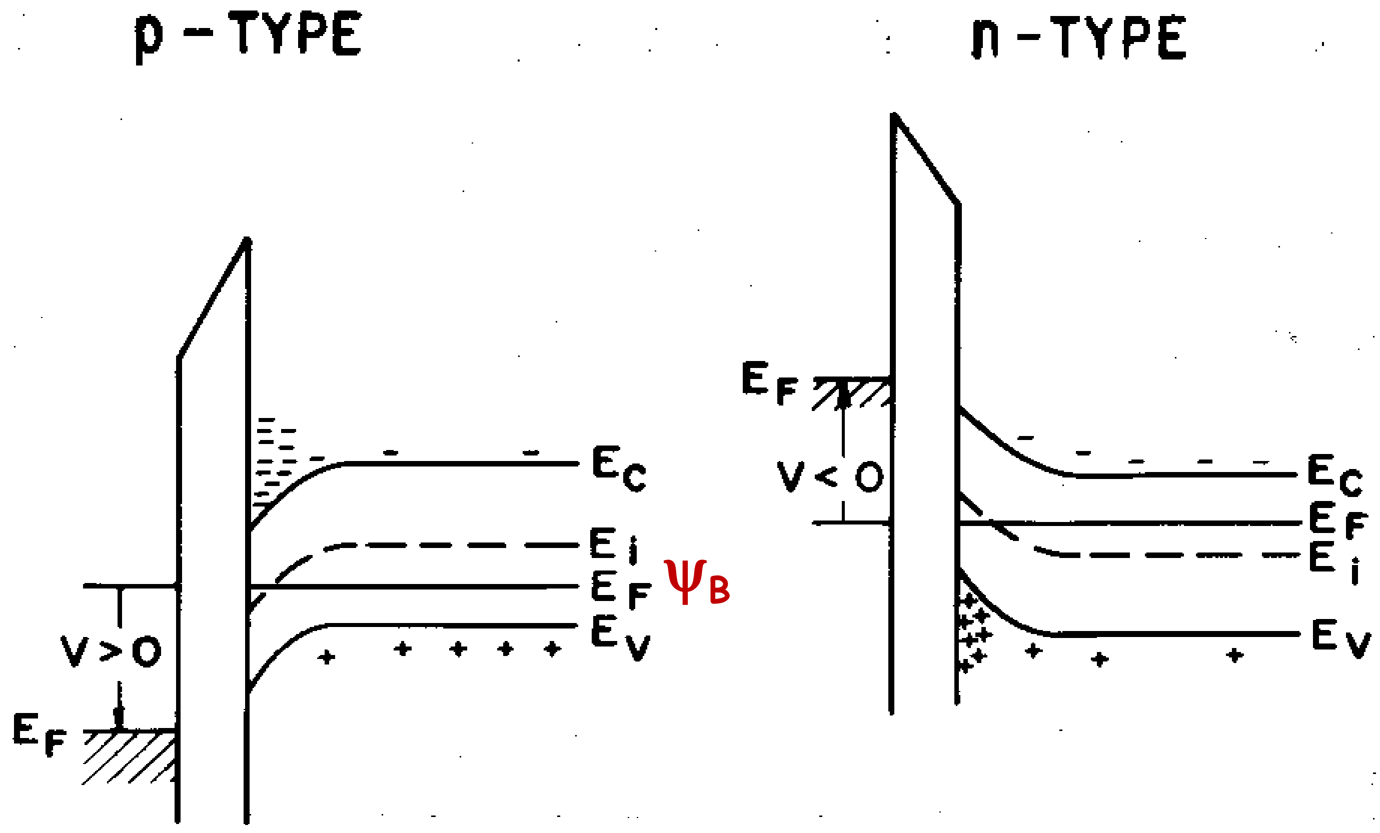
But this increases the barrier for current flow !!



Depletion



Inversion



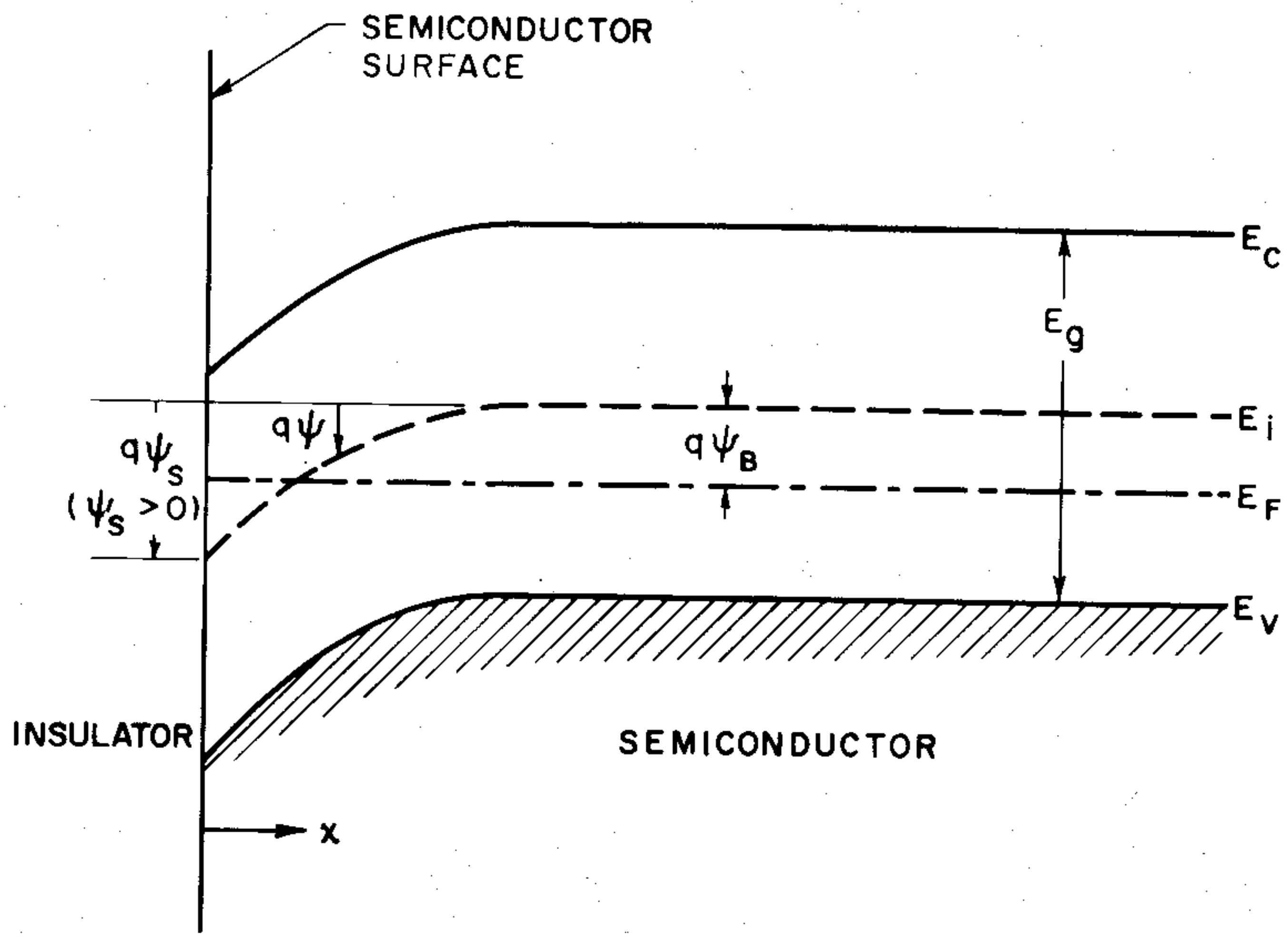
Need CB to dip below E_F.

Once below by ψ_B, minority carrier density trumps the intrinsic density.

Once below by $2\psi_B$, it trumps the major carrier density (doping) !

Sometimes maths <u>can</u> help…

P-type semiconductor $V_{appl} \neq 0$



Convention for p-type: ψ positive if bands bend down

Ideal MIS diode – p-type

$$n_p = n_i e^{-(E_i^{'}-E_F)/kT} = n_i e^{-(E_i - q\psi - E_F)/kT} = n_{p0} e^{q\psi/kT} = n_{p0} e^{\beta\psi}$$

CB moves towards E_F if $\psi > 0 \rightarrow$ n increases

$$p_p = p_{p0} e^{-q\psi/kT} = p_{p0} e^{-\beta\psi}$$

VB moves away from E_F if $\psi > 0 \rightarrow$ p decreases

$$\beta \equiv \frac{q}{kT}$$

Ideal MIS diode – p-type

At the semiconductor surface, $\psi = \psi_s$

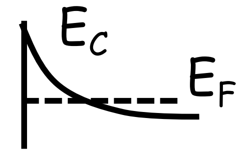
$$n_s = n_{p0} e^{\beta\psi_s}$$

$$p_s = p_{p0} e^{-\beta\psi_s}$$

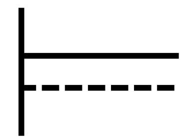
Surface carrier concentration

$$n_s = n_{p0} e^{\beta\psi_s} \qquad p_s = p_{p0} e^{-\beta\psi_s}$$

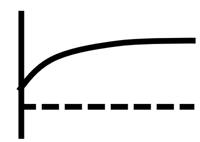
- $\psi_s < 0$ - accumulation of holes



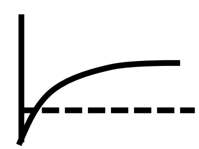
- $\psi_s = 0$ - flat band



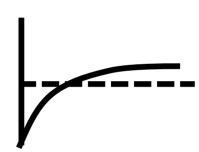
- $\psi_B > \psi_s > 0$ – depletion of holes



- $\psi_s = \psi_B$ - intrinsic concentration $n_s = p_s = n_i$



- $\psi_s > \psi_B$ – Inversion (more electrons than holes)



Want to find ψ, E-field, Capacitance

- Solve **Poisson's equation** to get E field, potential based on charge density distribution(one dimension)

$$\nabla \cdot \mathcal{E} = \rho / k\varepsilon_0 = \rho / \varepsilon_s = \frac{d\mathcal{E}}{dx} \rightarrow 1-D$$

$$\mathcal{E} = -\frac{d\psi}{dx}$$

$$\Rightarrow \frac{d^2\psi}{dx^2} = -\rho / \varepsilon_s$$

$$\rho(x) = q(N_D^+ - N_A^- + p_p - n_p)$$

- Away from the surface, $\rho = 0$

$$\Rightarrow N_D^+ - N_A^- = n_{p0} - p_{p0}$$

- and

$$p_p - n_p = p_{p0}e^{-\beta\psi} - n_{p0}e^{\beta\psi}$$

$$\Rightarrow \boxed{\frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_s}\left(p_{p0}\left(e^{-\beta\psi} - 1\right) - n_{p0}\left(e^{\beta\psi} - 1\right)\right)}$$

Solve Poisson's equation:

$$\Rightarrow \frac{d^2\psi}{dx^2} = -\frac{q}{\varepsilon_s}\left(p_{p0}(e^{-\beta\psi} - 1) - n_{p0}(e^{\beta\psi} - 1)\right)$$

$\mathcal{E} = -d\psi/dx$

$d^2\psi/dx^2 = -d\mathcal{E}/dx$

$= (d\mathcal{E}/d\psi).(-d\psi/dx)$

$= \mathcal{E}d\mathcal{E}/d\psi$

$$\mathcal{E}d\mathcal{E}/d\psi = -\frac{q}{\varepsilon_s}\left(p_{p0}(e^{-\beta\psi} - 1) - n_{p0}(e^{\beta\psi} - 1)\right)$$

Solve Poisson's equation:

- Do the integral:
- LHS:

$$\int_0^x x\,dx = \frac{x^2}{2} \rightarrow x = \frac{d\psi}{dx}$$

- RHS:

$$\int_0^x e^{\pm\beta x} dx, \int_0^x dx$$

- Get expression for $\mathcal{E}$ field (dψ/dx):

$$E_{field}^2 = \left(\frac{kT}{q}\right)^2 \left(\frac{qp_{p0}\beta}{2\varepsilon_s}\right)\left[\left(e^{-\beta\psi} + \beta\psi - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\beta\psi} - \beta\psi - 1\right)\right]$$

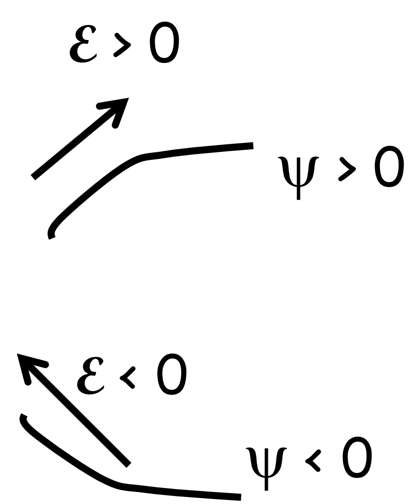
Define:

$$L_D \equiv \sqrt{\frac{kT\varepsilon_s}{p_{p0}q^2}} \equiv \sqrt{\frac{\varepsilon_s}{qp_{p0}\beta}}$$ Debye Length

$$F\left(\beta\psi,\frac{n_{p0}}{p_{p0}}\right)=\left[\left(e^{-\beta\psi}+\beta\psi-1\right)+\frac{n_{p0}}{p_{p0}}\left(e^{\beta\psi}-\beta\psi-1\right)\right]^{1/2}$$

Then:

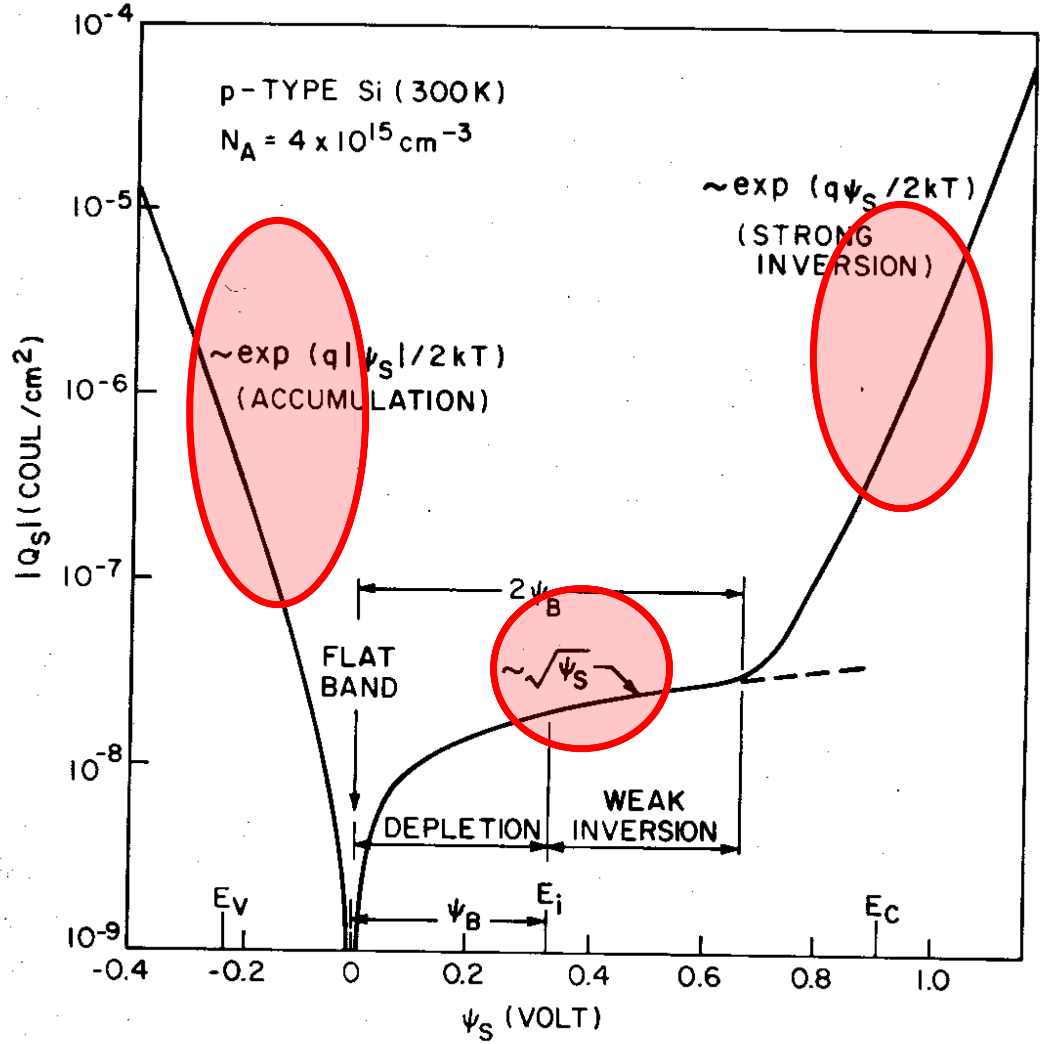
$$E_{field}=\pm\frac{\sqrt{2}kT}{qL_D}F\left(\beta\psi,\frac{n_{p0}}{p_{p0}}\right)$$



+ for $\psi > 0$ and – for $\psi < 0$

Use Gauss' Law to find surface charge per unit area

$$Q_s = -\varepsilon_s E_S = \mp \frac{\sqrt{2}kT}{qL_D} F\left(\beta\psi_s, \frac{n_{p0}}{p_{p0}}\right)$$



$$Q_s = \mp \frac{\sqrt{2}kT}{qL_D}\left[\left(e^{-\beta\psi_s} + \beta\psi_s - 1\right) + \frac{n_{p0}}{p_{p0}}\left(e^{\beta\psi_s} - \beta\psi_s - 1\right)\right]^{1/2}$$

Accumulation to depletion to strong Inversion

- For negative ψ, first term in F dominates – exponential
- For small positive ψ, second term in F dominates - $\sqrt{\psi}$
- As ψ gets larger, $\frac{n_{p0}e^{\beta\psi}}{p_{p0}} \rightarrow 1$ second exponential gets big

$$\psi_B = (kT/q)\ln(N_A/n_i) = (1/\beta)\ln(p_{p0}/\sqrt{p_{p0}n_{p0}})$$

$$(n_{p0}/p_{p0}) = e^{-2\beta\psi_B}$$

$$\psi_S > 2\psi_B$$

Questions

✓ What is the MOS capacitance? $Q_S(\psi_S)$

✓ What are the local conditions during inversion? $\psi_{S,cr}$

How does the potential vary with position? $\psi(x)$

How much inversion charge is generated at the surface? $Q_{inv}(x,\psi_S)$

Add in the oxide: how does the voltage divide? $\psi_S(V_G)$, $\psi_{ox}(V_G)$

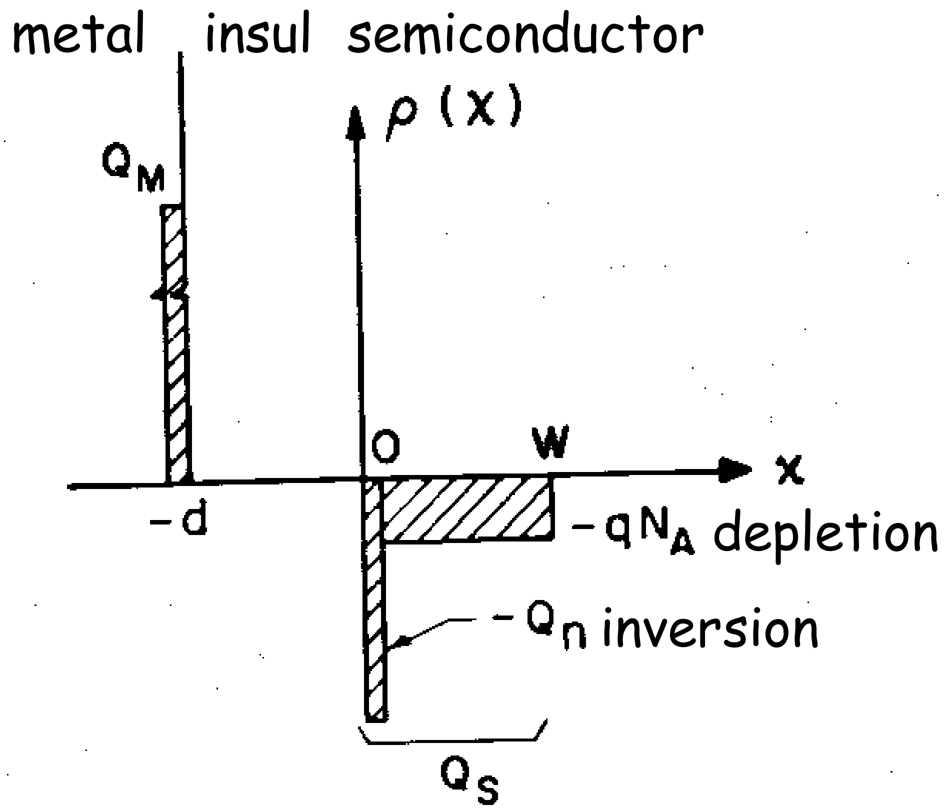
How much gate voltage do you need to invert the channel? V_{TH}

How much inversion charge is generated by the gate? $Q_{inv}(V_G)$

What's the overall C-V of the MOSFET? $Q_S(V_G)$

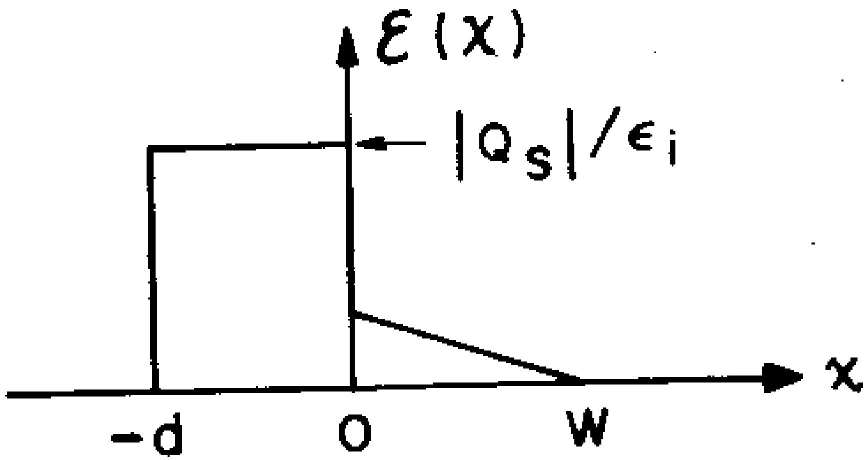
Charges, fields, and potentials

- Charge on metal = induced surface charge in semiconductor
- No charge/current in insulator (ideal)

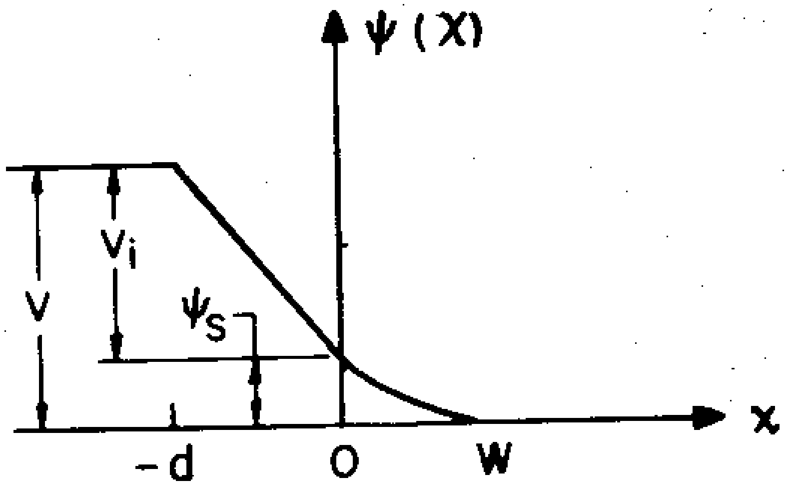


$$Q_M = Q_n + qN_A W = Q_S$$

Charges, fields, and potentials

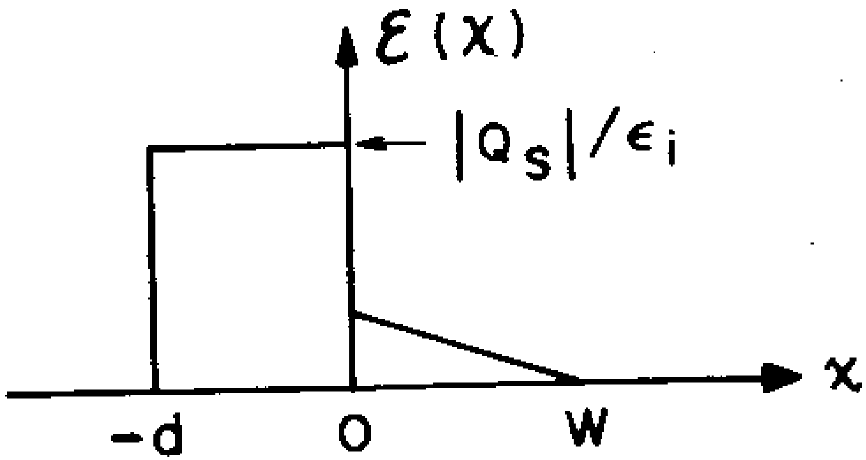


Electric Field

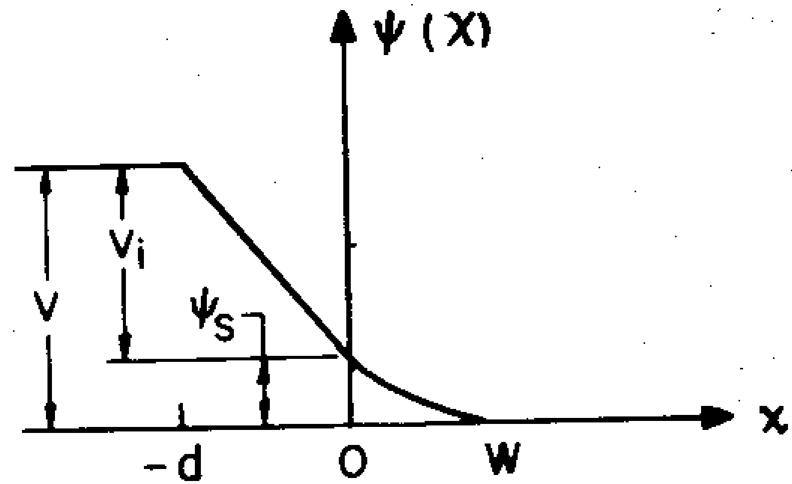


Electrostatic Potential

Depletion Region



Electric Field



Electrostatic Potential

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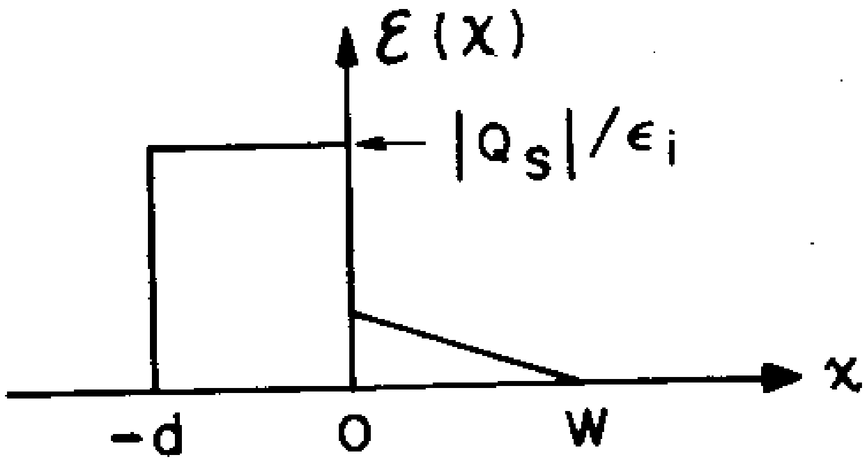
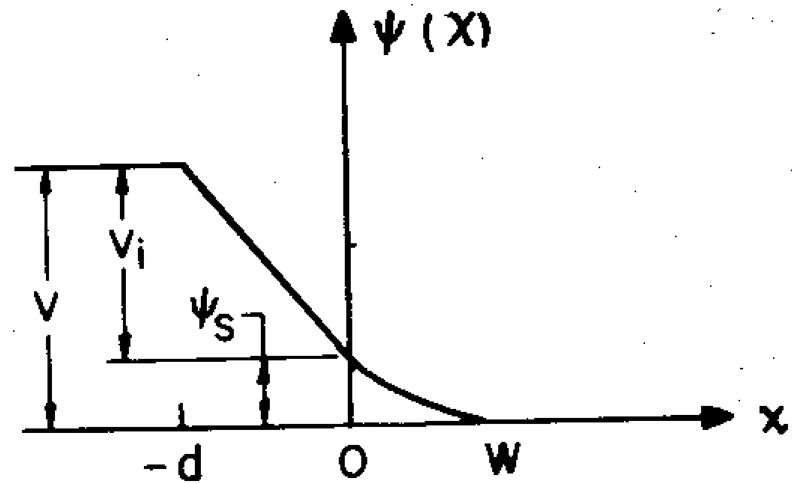
Depletion Region



Electric Field



Electrostatic Potential

$$\psi = \psi_s(1\text{-}x/W)^2$$

$$W_{max} = \sqrt{2\varepsilon_s(2\psi_B)/qN_A}$$

$$\psi_B = (kT/q)\ln(N_A/n_i)$$

Questions

- ✓ What is the MOS capacitance? $Q_S(\psi_S)$
- ✓ What are the local conditions during inversion? $\psi_{S,cr}$
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What's the overall C-V of the MOSFET? $Q_S(V_G)$

Couldn't we just solve this exactly?

Exact Solution

$$U = \beta\psi$$

$$U_S = \beta\psi_S$$

$$U_B = \beta\psi_B$$

$$d\psi/dx = -(\sqrt{2kT}/qL_D)F(\psi_B, n_{p0}/p_{p0})$$

$$\int_{U_S}^{U} dU/F(U) = \pm\, x/L_D$$

$$F(U) = [e^{U_B}(e^{-U}-1+U)-e^{-U_B}(e^{U}-1-U)]^{1/2}$$

Exact Solution

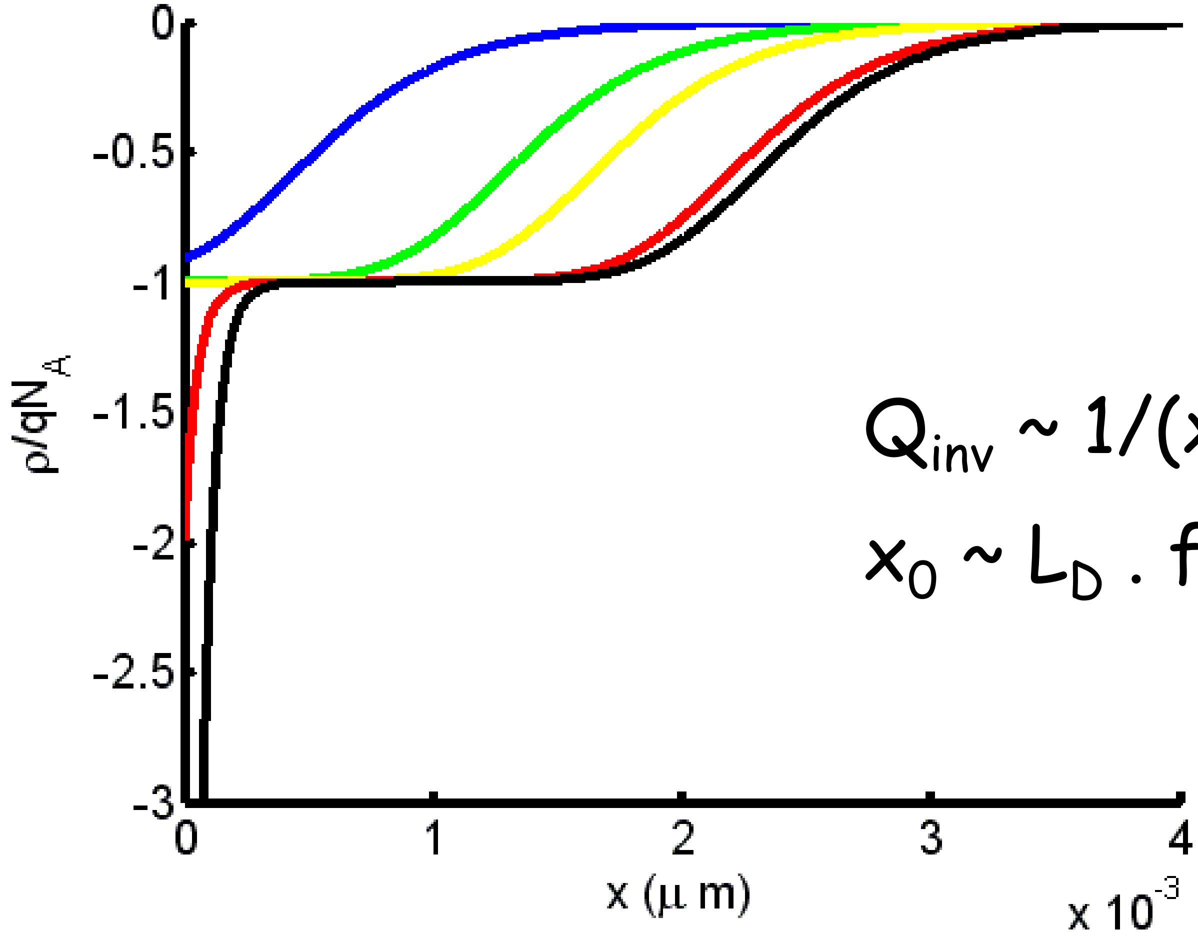
$$\rho = qn_i[e^{U_B}(e^{-U}-1) - e^{-U_B}(e^{U}-1)]$$

$$\int_{U}^{U_S} dU'/F(U',U_B) = \pm\, x/L_D$$

$$F(U,U_B) = [e^{U_B}(e^{-U}-1+U) + e^{-U_B}(e^{U}-1-U)]^{1/2}$$

Exact Solution

$N_A = 1.67 \times 10^{15}$



$Q_{inv} \sim 1/(x+x_0)^{\alpha}$

$x_0 \sim L_D$. factor

Questions

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Threshold Voltage for Strong Inversion

- Total voltage across MOS structure= voltage across dielectric plus ψ_s

$$V_T(strong\_inversion) = V_i + \psi_S = \frac{Q_S}{C_i} + 2\psi_B$$

$$Q_S(SI) = qN_A W_{\max} = qN_A \sqrt{\frac{2\varepsilon_s \psi_s(inv)}{qN_A}} = \sqrt{2\varepsilon_s qN_A(2\psi_B)}$$

$$\Rightarrow V_T = \frac{\sqrt{2\varepsilon_s qN_A(2\psi_B)}}{C_i} + 2\psi_B$$

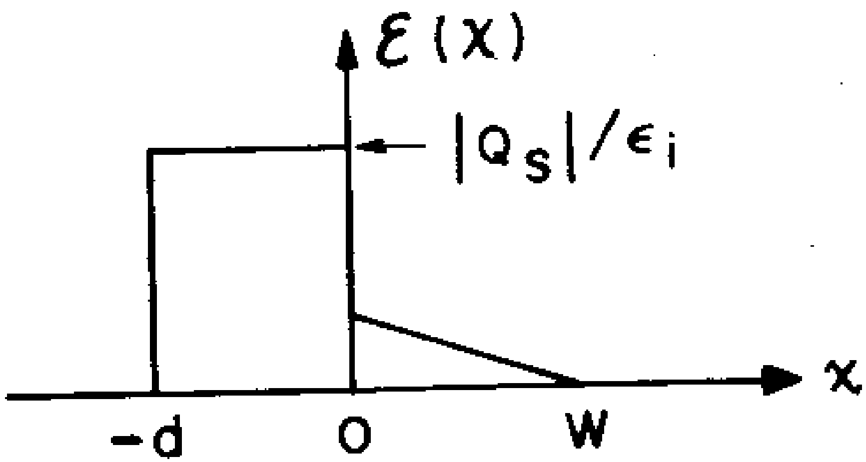
Notice Boundary Condition !!

$\varepsilon_{ox} V_i / t_{ox} = \varepsilon_s \psi_s / (W/2)$ Before Inversion

After inversion there is a discontinuity in D due to surface Q_{inv}

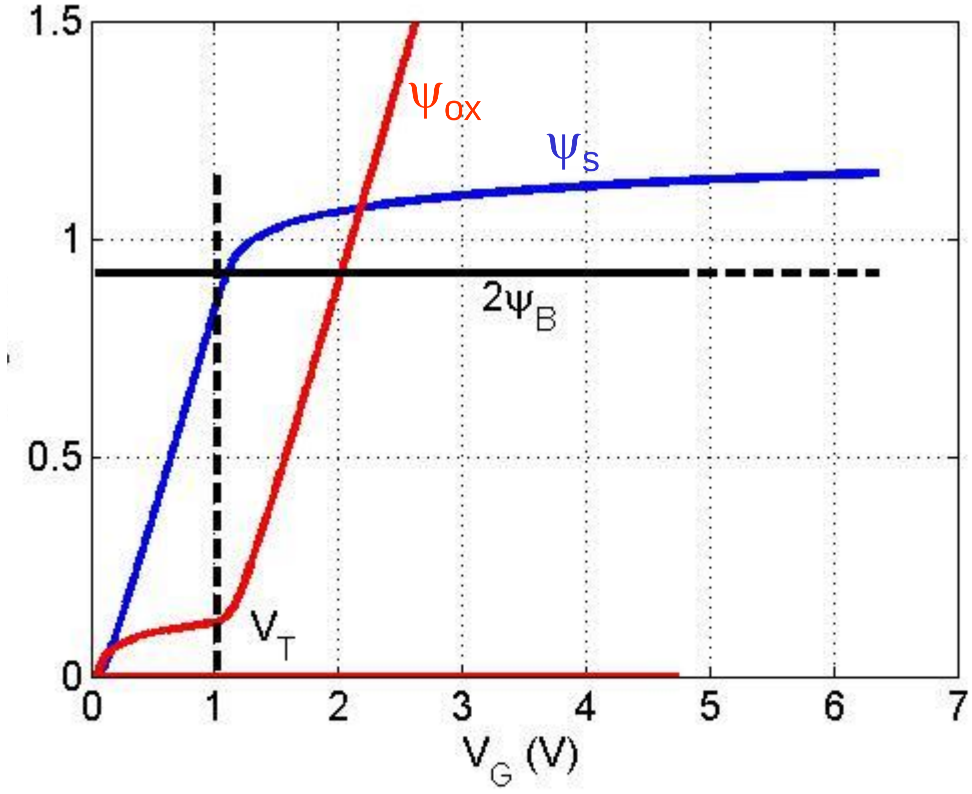
V_{ox} (at threshold) = $\varepsilon_s (2\psi_B)/(W_{max}/2) C_i$ =

$$= \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_i}$$



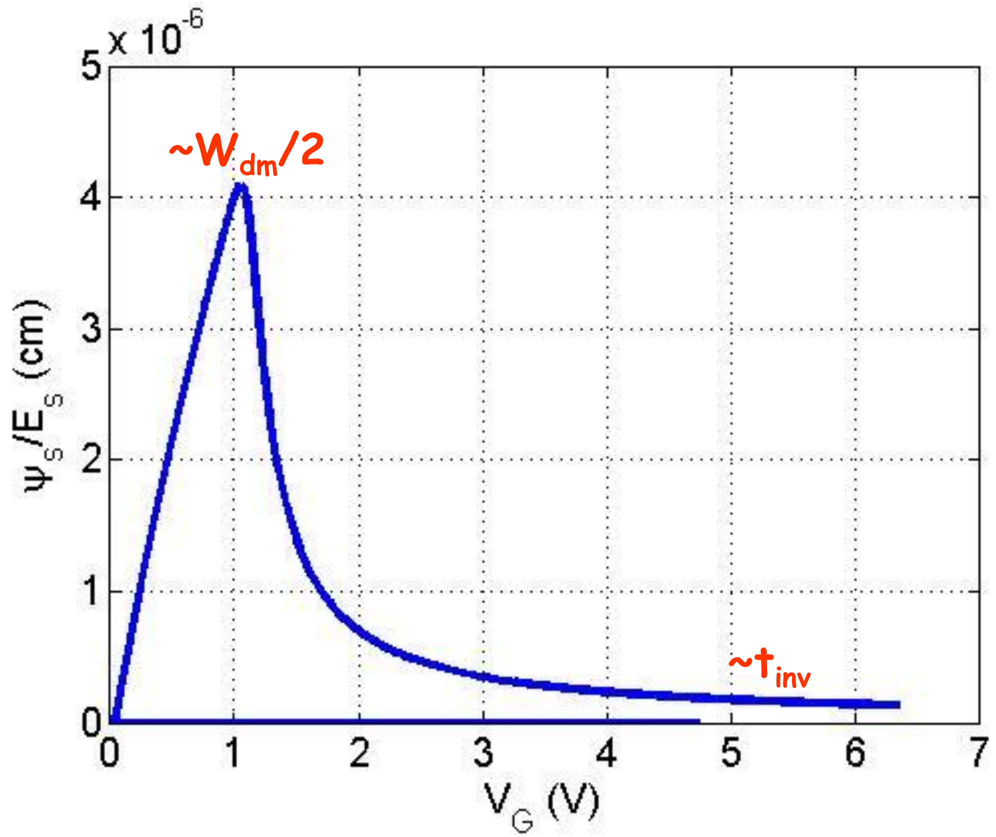
Local Potential vs Gate voltage

$$V_G = V_{fb} + \psi_s + (\kappa_s t_{ox}/\kappa_{ox})\sqrt{(2kTN_A/\varepsilon_0\kappa_s)}[\beta\psi_s + e^{\beta(\psi_s - 2\psi_B)}]^{1/2}$$



Initially, all voltage drops across channel (blue curve). Above threshold, channel potential stays pinned to $2\psi_B$, varying only logarithmically, so that most of the gate voltage drops across the oxide (red curve).

Look at Effective charge width



Initially, a fast increasing channel potential drops across increasing depletion width

Eventually, a constant potential drops across a decreasing inversion layer width, so field keeps increasing and thus matches increasing field in oxide

Questions

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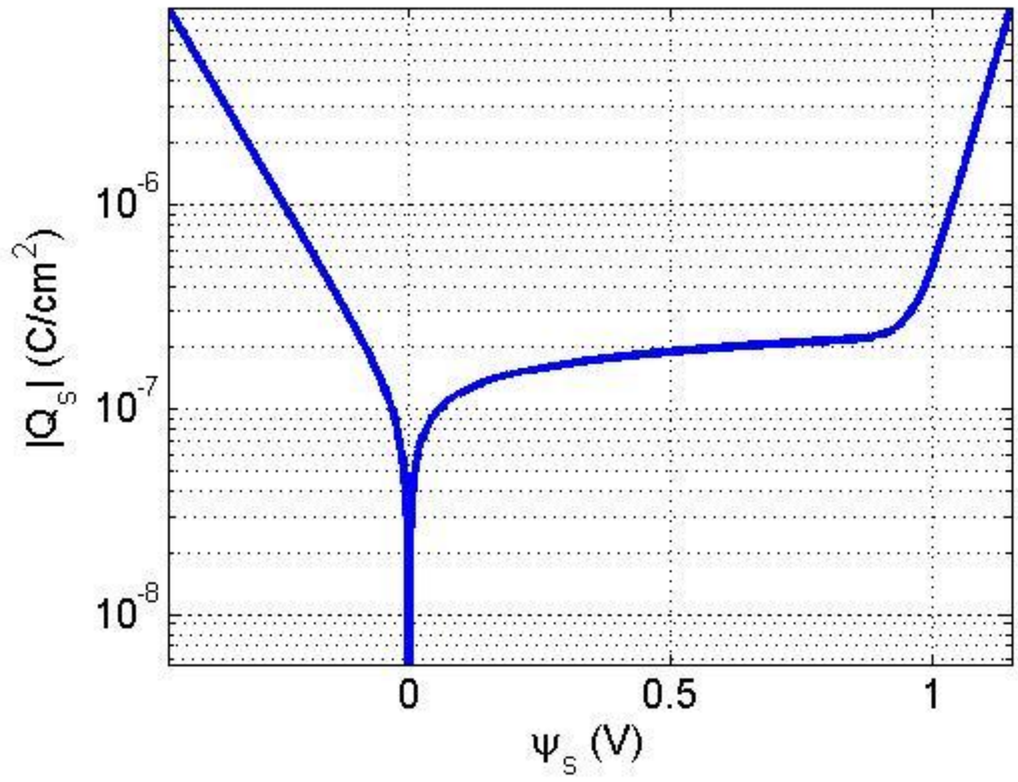
- ✓ Add in the oxide: how does the voltage divide? $\psi_S(V_G)$, $\psi_{ox}(V_G)$
- ✓ How much gate voltage do you need to invert the channel? V_{TH}

How much inversion charge is generated by the gate? $Q_{inv}(V_G)$

What's the overall C-V of the MOSFET? $Q_S(V_G)$

Charge vs Local Potential

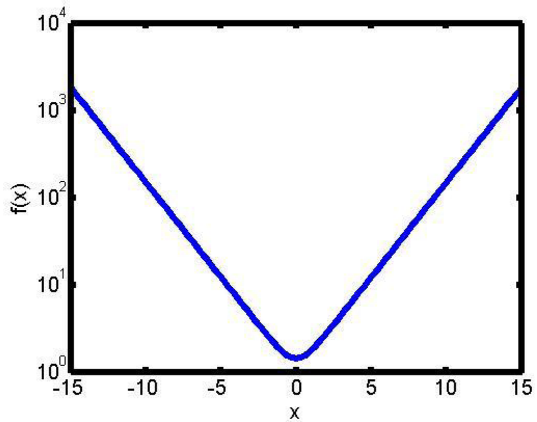
$$Q_s \approx \sqrt{(2\varepsilon_0\kappa_s kTN_A)}[\beta\psi_s + e^{\beta(\psi_S-2\psi_B)}]^{1/2}$$



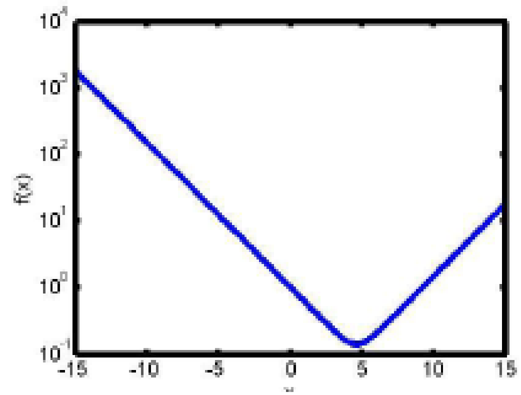
Beyond threshold, all charge goes to inversion layer

NEW

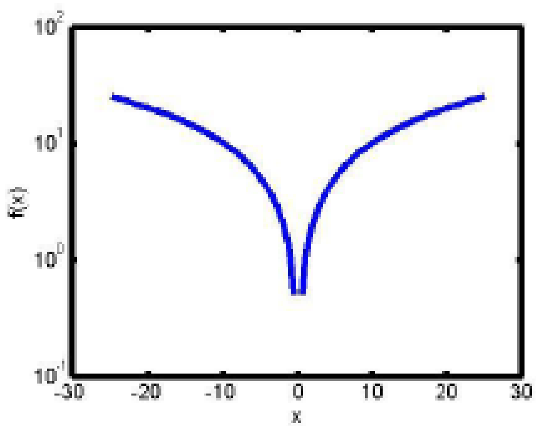
How do we get the curvatures?



$[\exp(-\beta x) + n_r.\exp(\beta x)]^{1/2}$ with $n_r = 1$.

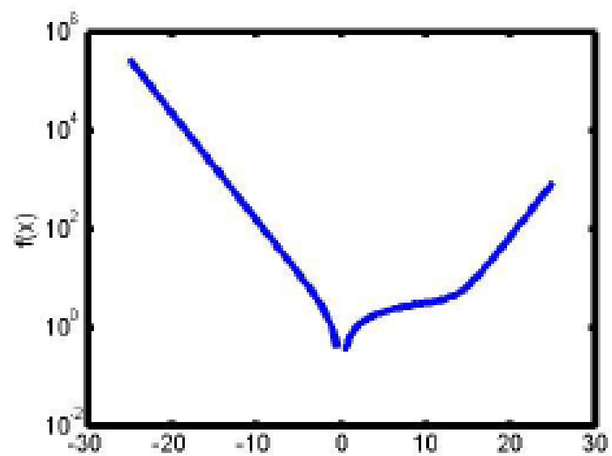


$n_r = 10^{-3}$.



Add other terms and keep Leading term

$(x^2 + n_r.[\, x^2])^{1/2}$



EXACT

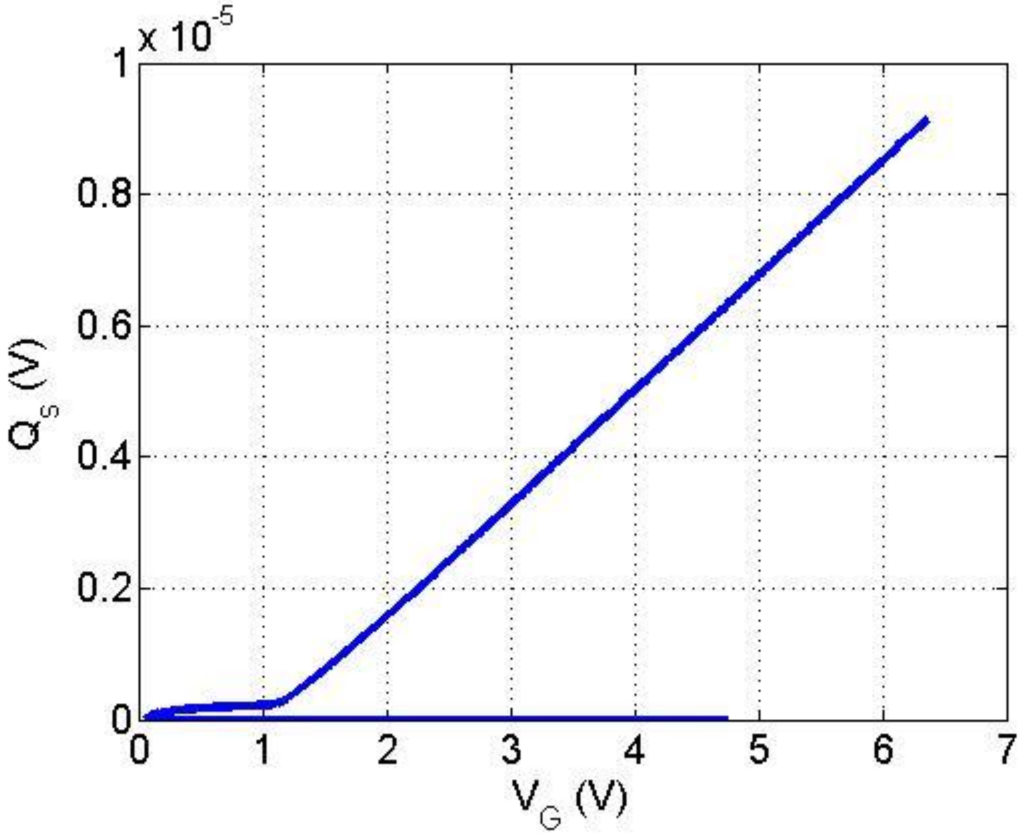
$([\exp(-\beta x) + \beta x - 1) + n_r.[\exp(\beta x) - \beta x - 1])^{1/2}$

Inversion Charge vs Gate voltage

$Q \sim e^{\beta(\psi_s - 2\psi_B)}$, $\psi_s - 2\psi_B \sim \log(V_G - V_T)$

Exponent of a logarithm gives a linear variation of Q_{inv} with V_G

$$Q_{inv} = -C_{ox}(V_G - V_T)$$



Why C_{ox}?

Questions

- ✓ What is the MOS capacitance? $Q_S(\psi_S)$
- ✓ What are the local conditions during inversion? $\psi_{S,cr}$
- ✓ How does the potential vary with position? $\psi(x)$
- ✓ How much inversion charge is generated at the surface? $Q_{inv}(x,\psi_S)$
- ✓ Add in the oxide: how does the voltage divide? $\psi_S(V_G)$, $\psi_{ox}(V_G)$
- ✓ How much gate voltage do you need to invert the channel? V_{TH}
- ✓ How much inversion charge is generated by the gate? $Q_{inv}(V_G)$

What's the overall C-V of the MOSFET? $Q_S(V_G)$

Capacitance

$$C_D = \frac{\partial Q_S}{\partial \psi} = \frac{\varepsilon_S}{\sqrt{2}L_D} \frac{\left[1 - e^{-\beta\psi_s} + \left({n_{p0}}/{p_{p0}} \right)\left(e^{-\beta\psi_s} - 1\right)\right]}{F\left(\beta\psi_S, \frac{n_{p0}}{p_{p0}}\right)}$$

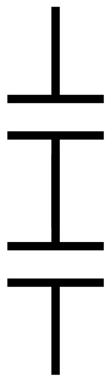
For ψ_s=0 (Flat Band):

Expand exponentials..... $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots\ldots..$

$$C_D(flat\_band) = \frac{\varepsilon_S}{L_D}$$

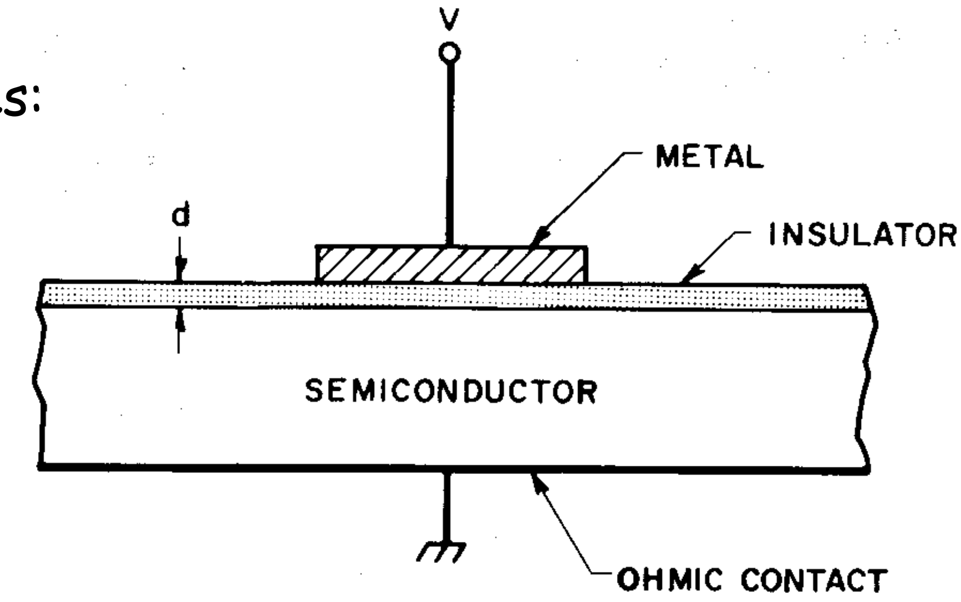
Capacitance of whole structure

- Two capacitors in series:



C_i - insulator

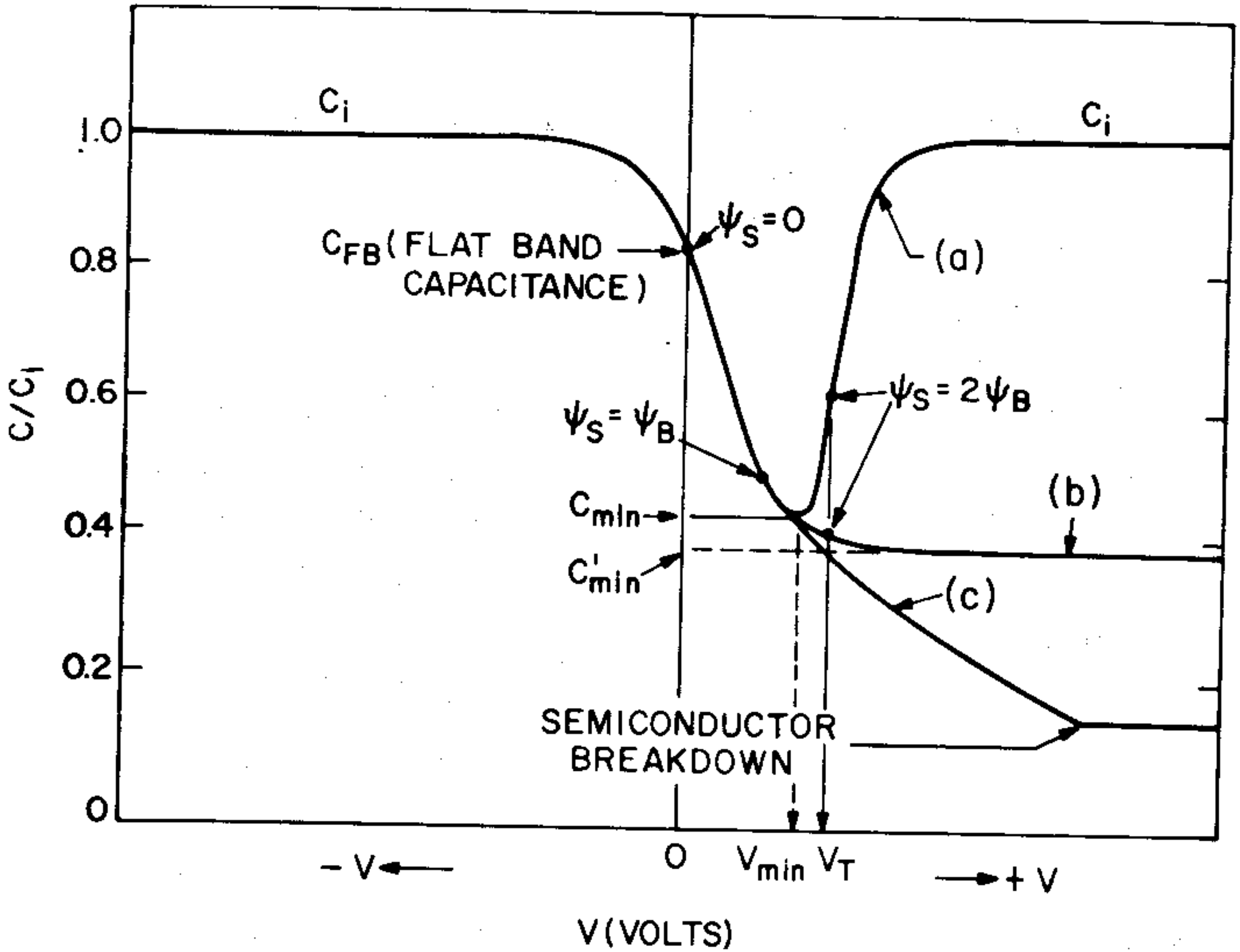
C_D - Depletion



$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_D} \qquad \text{OR} \qquad C = \frac{C_i C_D}{C_i + C_D}$$

$$C_i \equiv \frac{\varepsilon_i}{d}$$

Capacitance vs Voltage



Flat Band Capacitance

- Negative voltage = accumulation – $C \sim C_i$
- Zero voltage – Flat Band

$$V = 0 \Rightarrow \psi = 0 \Rightarrow C = C_{FB}$$

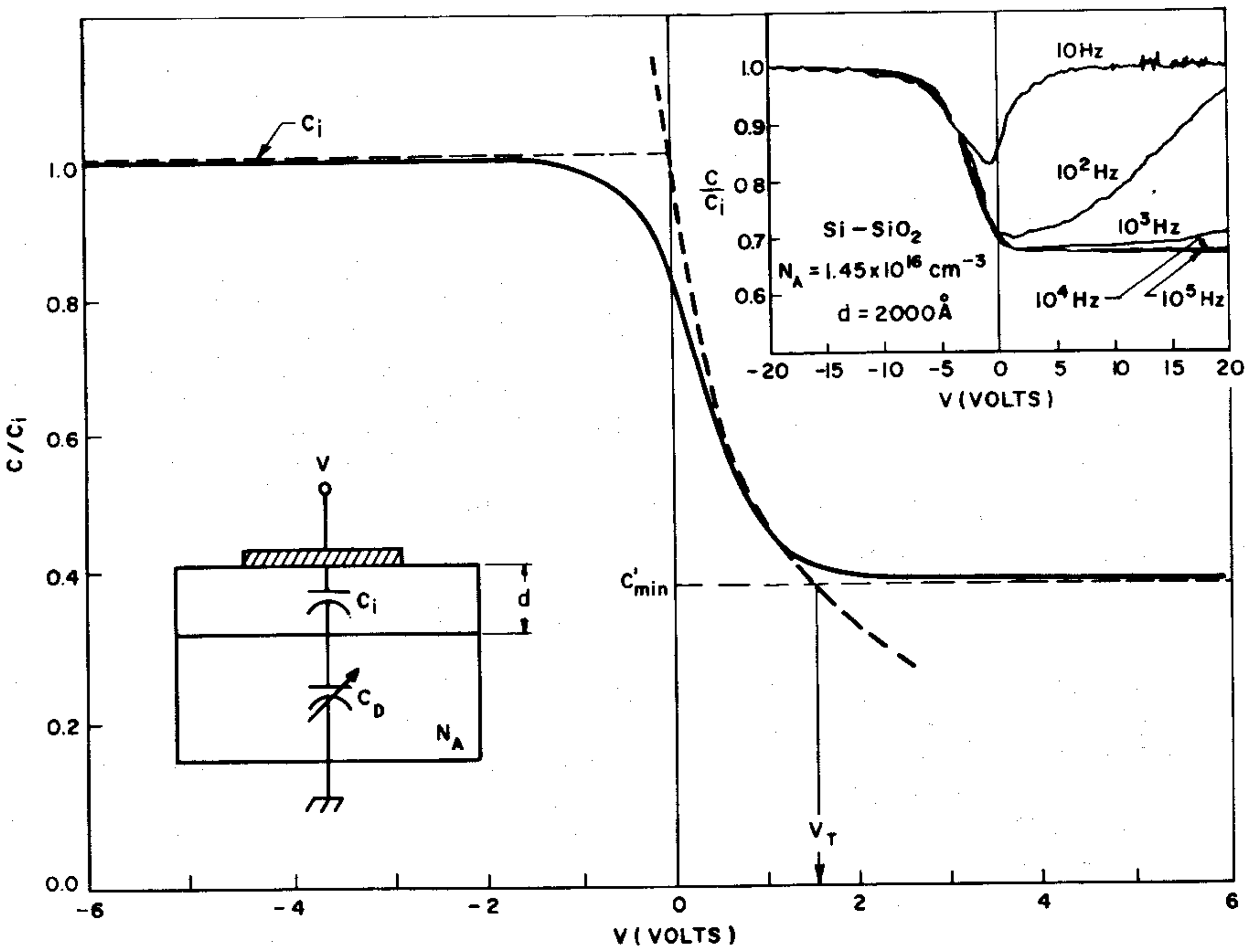
$$\frac{1}{C_{FB}} = \frac{1}{C_i} + \frac{1}{C_D} = \frac{1}{\frac{\varepsilon_i}{d}} + \frac{1}{\frac{\varepsilon_s}{L_D}} = \frac{\varepsilon_s d + \varepsilon_i L_D}{\varepsilon_i \varepsilon_s} = \frac{\dfrac{d + \frac{\varepsilon_i}{\varepsilon_s} L_D}{\varepsilon_s}}{\varepsilon_i}$$

$$\Rightarrow C_{FB} = \frac{\varepsilon_i}{d + \frac{\varepsilon_i}{\varepsilon_s} L_D}$$

CV

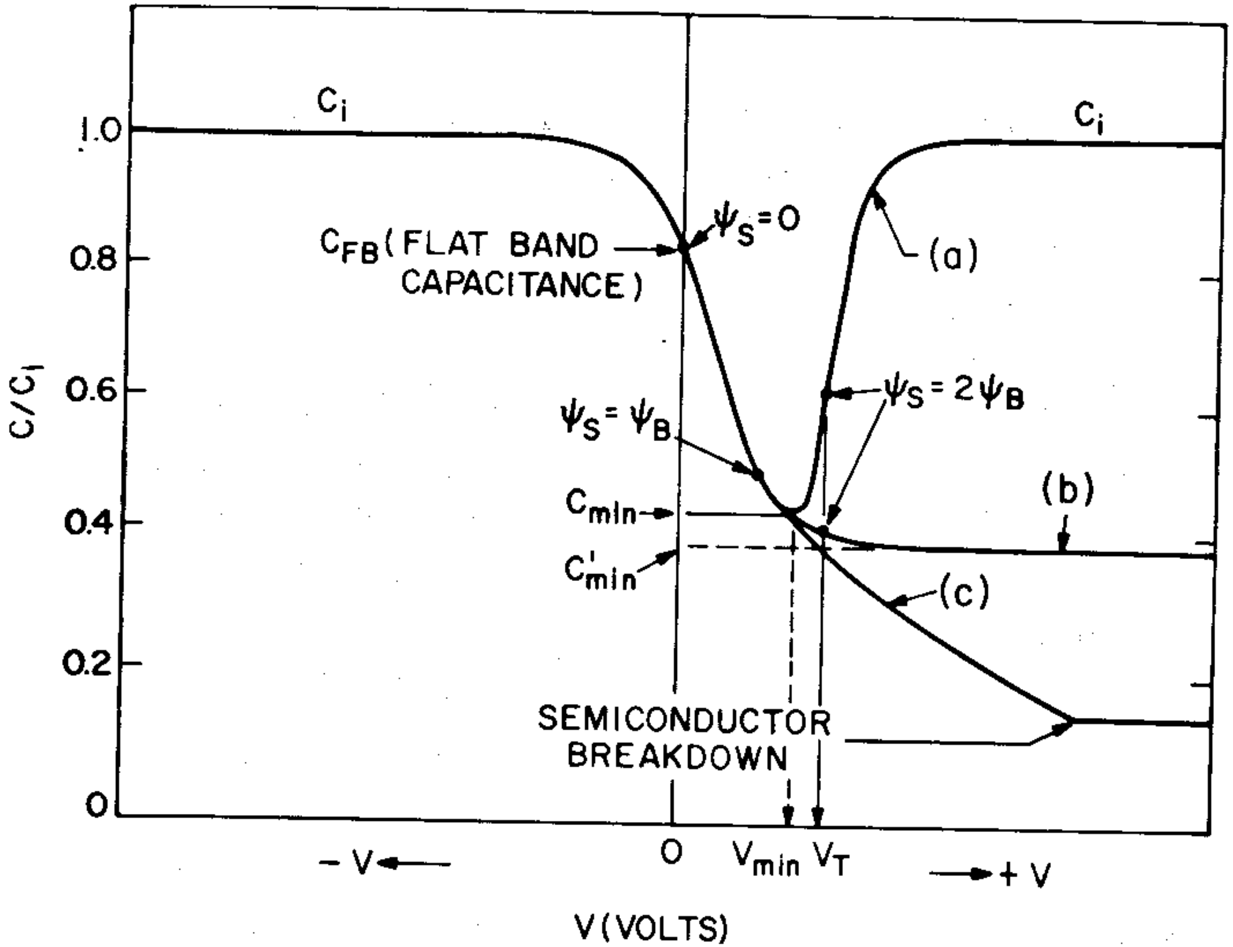
- As voltage is increased, C goes through minimum (weak inversion) where $d\psi/dQ$ is fairly flat
- C will increase with onset of strong inversion
- Capacitance is an AC measurement
- Only increases when AC period long wrt minority carrier lifetime
- At "high" frequency, carriers can't keep up – don't see increased capacitance with voltage
- For Si MOS, "high" frequency = 10-100 Hz

CV Curves – Ideal MOS Capacitor

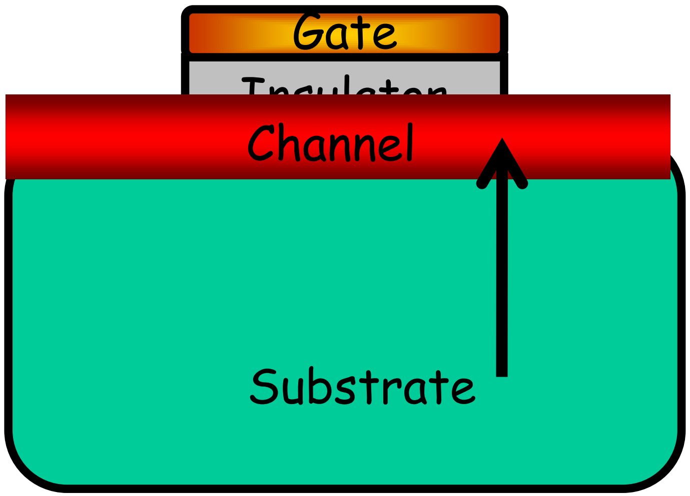


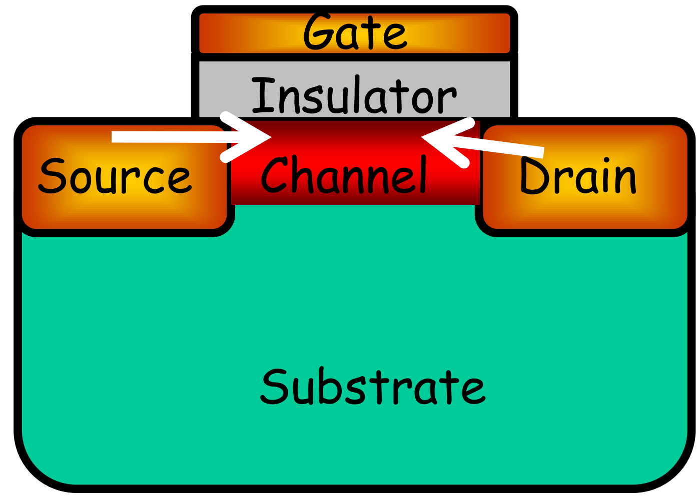
$$C'_{min} = \frac{\varepsilon_i}{d + \frac{\varepsilon_i}{\varepsilon_s} W_{max}}$$

MOScap vs MOSFET



MOScap vs MOSFET





Minority carriers generated by RG, over minority carrier lifetime ~ 100μs

So C_{inv} can be << C_{ox} if fast gate switching (~ GHz)

Majority carriers pulled in from contacts (fast !!)

$C_{inv} = C_{ox}$

Example Metal-SiO_2-Si

- $N_A = 10^{17}/cm^3$
- At room temp $kT/q = 0.026V$
- $n_i = 9.65x10^9/cm^3$
- $\varepsilon_s = 11.9x1.85x10^{-14}$ F/cm

$$W_{\max} = \sqrt{\frac{4\varepsilon_s kT \ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}} = \sqrt{\frac{11.9x8.85x10^{-14} X 0.026 \ln\left(10^{17}/9.65x10^9\right)}{1.6x10^{-19} X 10^{17}}}$$

$$W_{\max} = 10^{-5} cm = 0.1 \mu m$$

Example Metal-SiO_2-Si

- d=50 nm thick oxide=10^{-5} cm
- ε_i=3.9x8.85x10^{-14} F/cm

$$C_i = \frac{\varepsilon_i}{d} = \frac{3.9x8.85x10^{-14}}{10^{-5}} = 6.9x10^{-7} F/cm^2$$

$$\psi_s(inv) = 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) = 2x0.026x\ln\left(\frac{10^{17}}{9.65x10^9}\right) = 0.84 Volts$$

$$C'_{\min} = \frac{\varepsilon_i}{d + \frac{\varepsilon_i}{\varepsilon_s}W_{\max}} = \frac{3.9x8.85x10^{-14}}{5x10^{-7} + (3.9/11.9)10^{-5}} = 9.1x10^{-8} F/cm^2$$

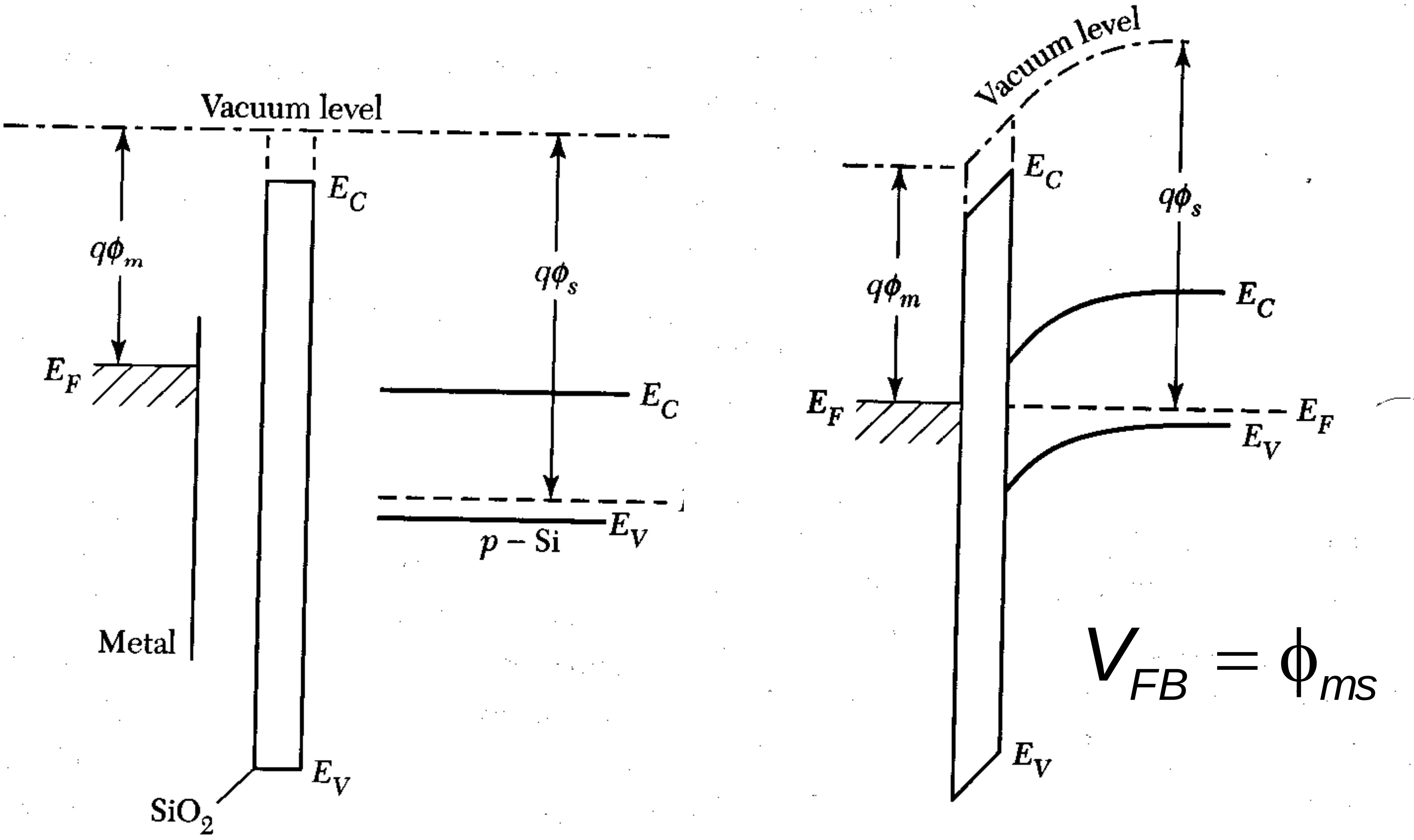
$$\frac{C'_{\min}}{C_i} = 0.13$$

$$V_{TH} = \frac{qN_A W_{\max}}{C_i} + 2\psi_B = \frac{1.6x10^{-19}x10^{17}x10^{-5}}{6.9x10^{-7}} + \psi_s(inv) = 0.23 + 0.84 = 1.07 Volts$$

Real MIS Diode: Metal(poly)-Si-SiO_2 MOS

- Work functions of gate and semiconductor are NOT the same
- Oxides are not perfect
  - Trapped, interface, mobile charges
  - Tunneling
- All of these will effect the CV characteristic and threshold voltage

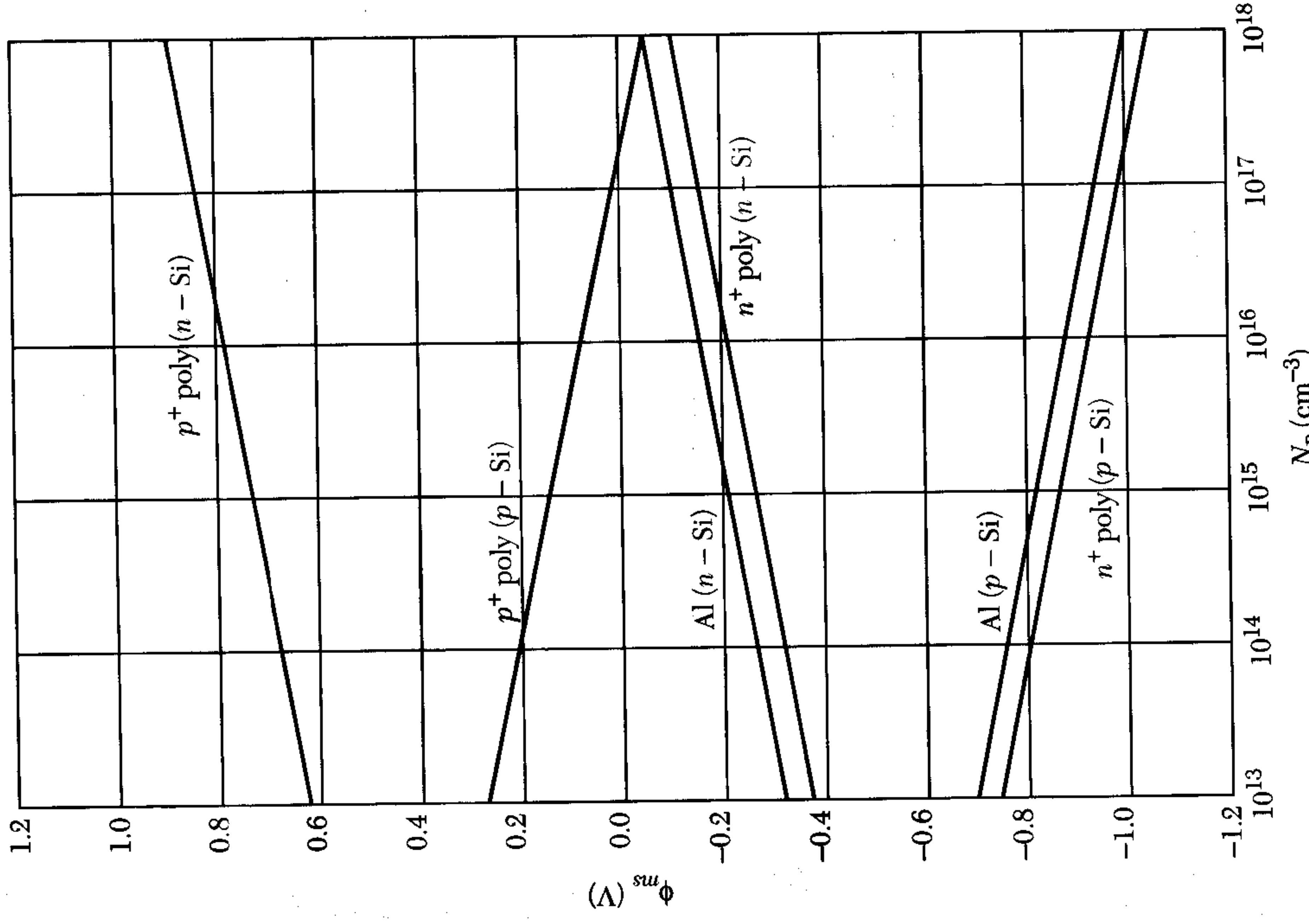
Band bending due to work function difference



$$V_{FB} = \phi_{ms}$$

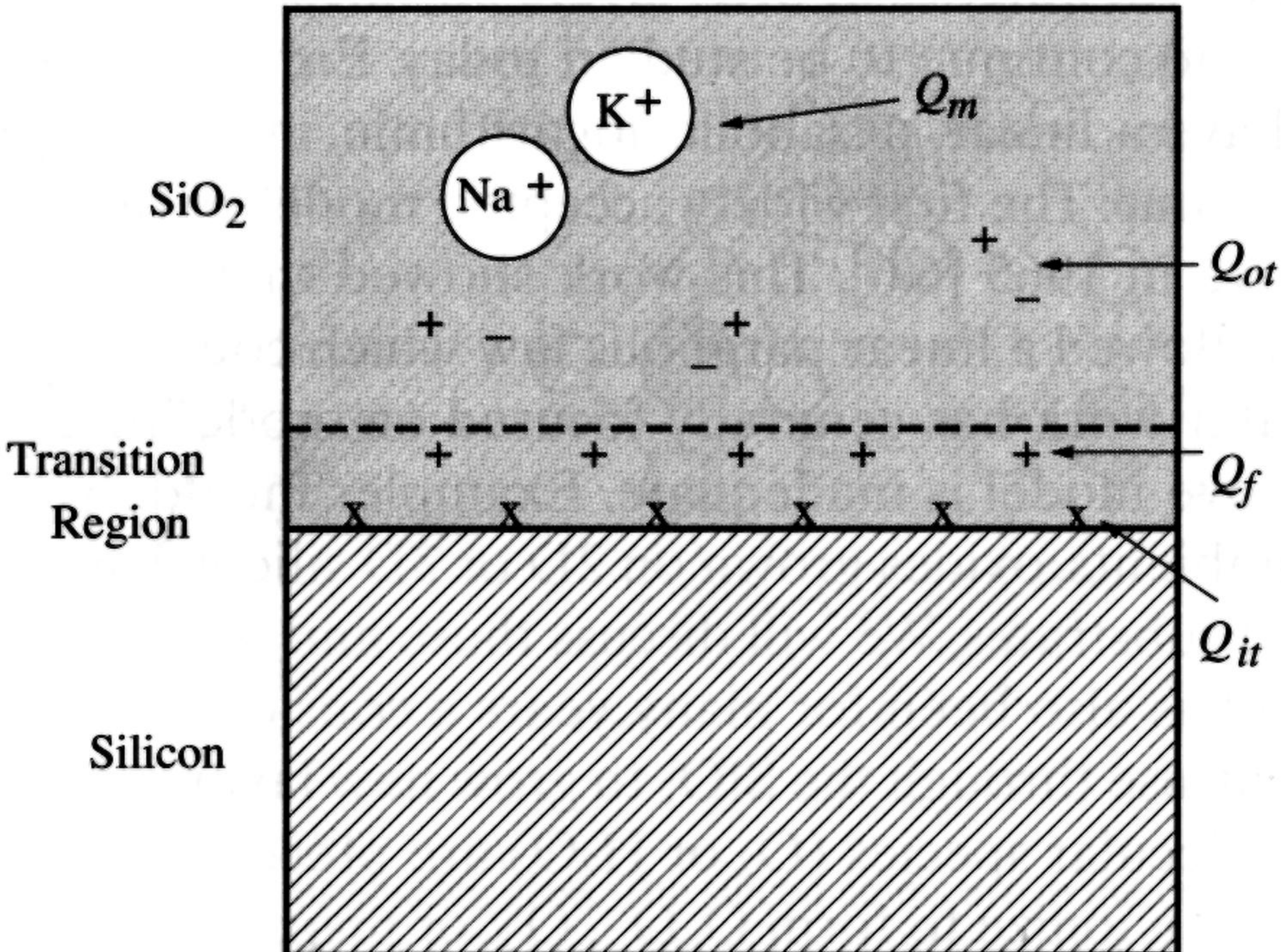
Work Function Difference

- $q\phi_s$=semiconductor work function = difference between vacuum and Fermi level
- $q\phi_m$=metal work function
- $q\phi_{ms}=(q\phi_m - q\phi_s)$
- For Al, $q\phi_m$=4.1 eV
- n^+ polysilicon $q\phi_s$=4.05 eV
- p^+ polysilicon $q\phi_s$=5.05 eV
- $q\phi_{ms}$ varies over a wide range depending on doping



p^+ poly $(n-$Si)
p^+ poly $(p-$Si)
Al $(n-$Si)
n^+ poly $(n-$Si)
Al $(p-$Si)
n^+ poly $(p-$Si)
ϕ_{ms} (V)
N_B (cm^{-3})
1.2
1.0
0.8
0.6
0.4
0.2
0.0
−0.2
−0.4
−0.6
−0.8
−1.0
−1.2
10^{13}
10^{14}
10^{15}
10^{16}
10^{17}
10^{18}

SiO_2-Si Interface Charges



Standard nomenclature for Oxide charges:

Q_M=Mobile charges (Na+/K+) – can cause unstable threshold shifts – cleanliness has eliminated this issue

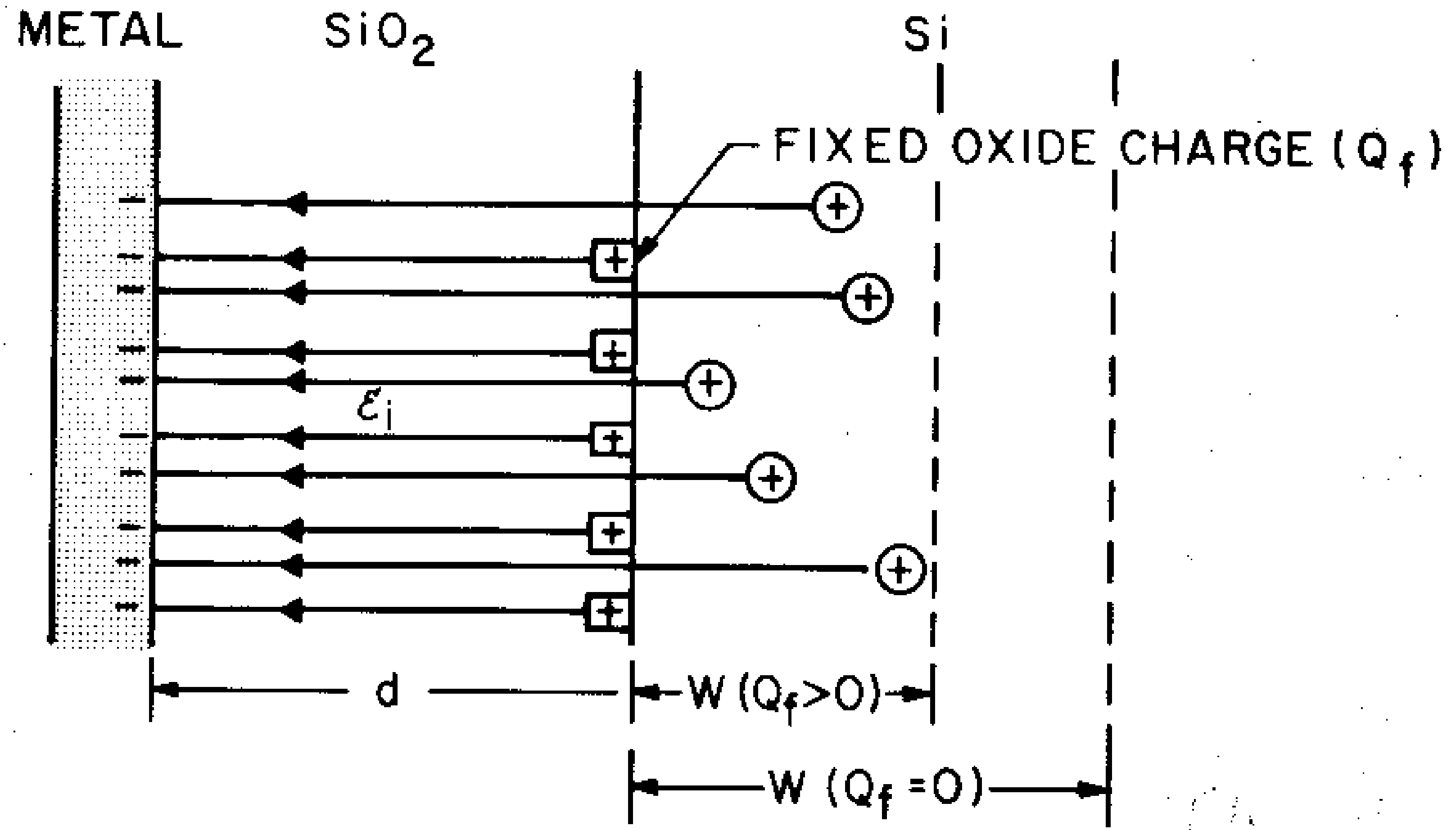
Q_{OT}=Oxide trapped charge – Can be anywhere in the oxide layer. Caused by broken Si-O bonds – caused by radiation damage e.g. alpha particles, plasma processes, hot carriers, EPROM

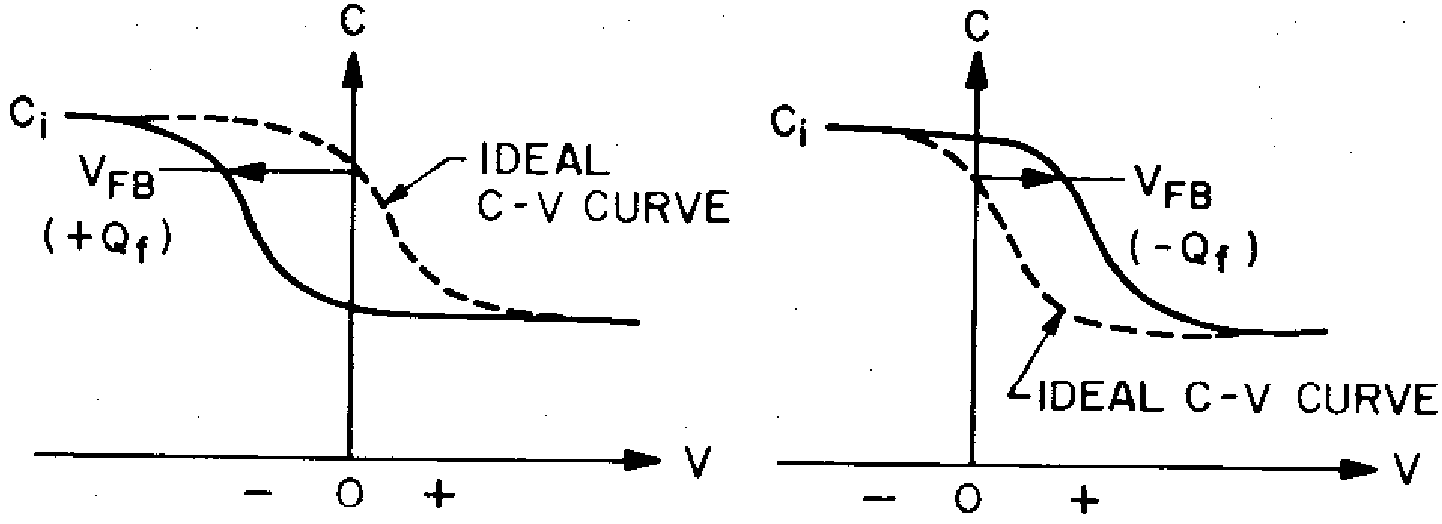
Q_F= Fixed oxide charge – positive charge layer near (~2mm) Caused by incomplete oxidation of Si atoms(dangling bonds) Does not change with applied voltage

Q_{IT}=Interface trapped charge. Similar in origin to Q_F but at interface. Can be pos, neg, or neutral. Traps e^- and h during device operation. Density of Q_{IT} and Q_F usually correlated-similar mechanisms. Cure is H anneal at the end of the process.

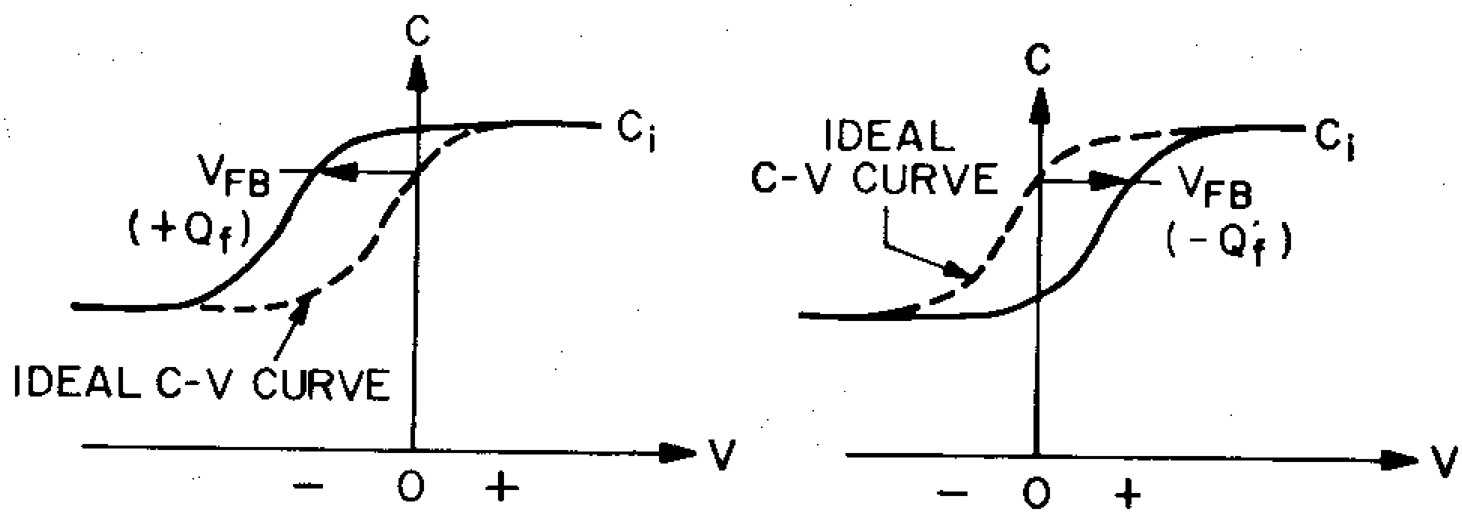
Oxide charges measured with C-V methods

Effect of Fixed Oxide Charges

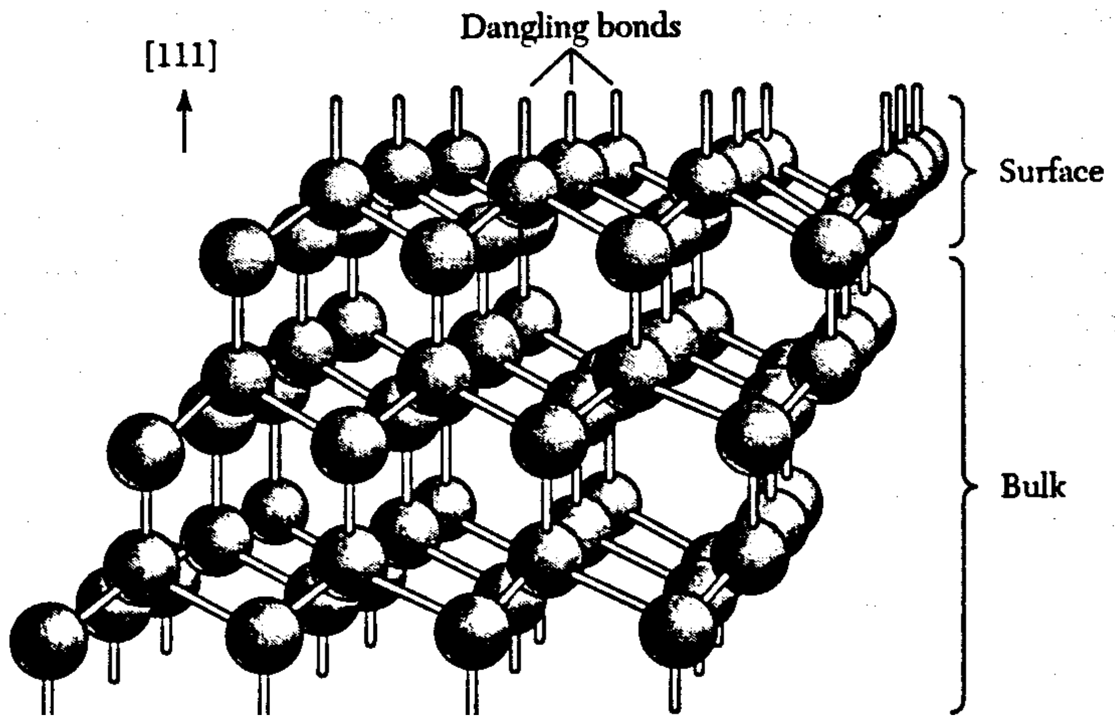



C
C
C_i
C_i
V_{FB}
$(+Q_f)$
IDEAL
C-V CURVE
V_{FB}
$(-Q_f)$
IDEAL C-V CURVE
V
V
− 0 +
− 0 +

(a)


C
C
C_i
C_i
V_{FB}
$(+Q_f)$
IDEAL C-V CURVE
IDEAL
C-V CURVE
V_{FB}
$(-Q_f')$
V
V
− 0 +
− 0 +

Surface Recombination



Lattice periodicity broken at surface/interface – mid-gap E levels
Carriers generated-recombined per unit area

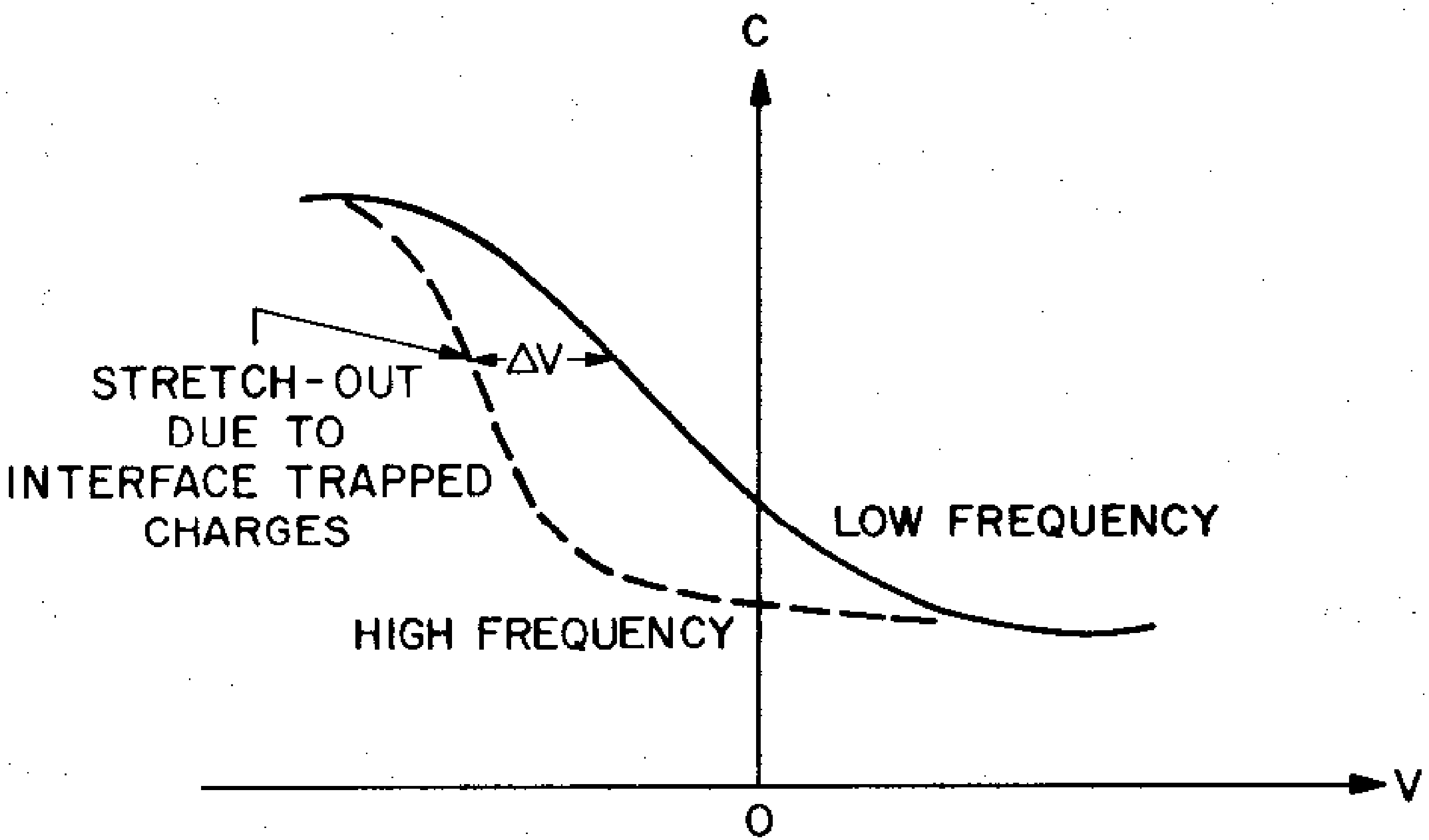
Interface Trapped Charge - Q_{IT}

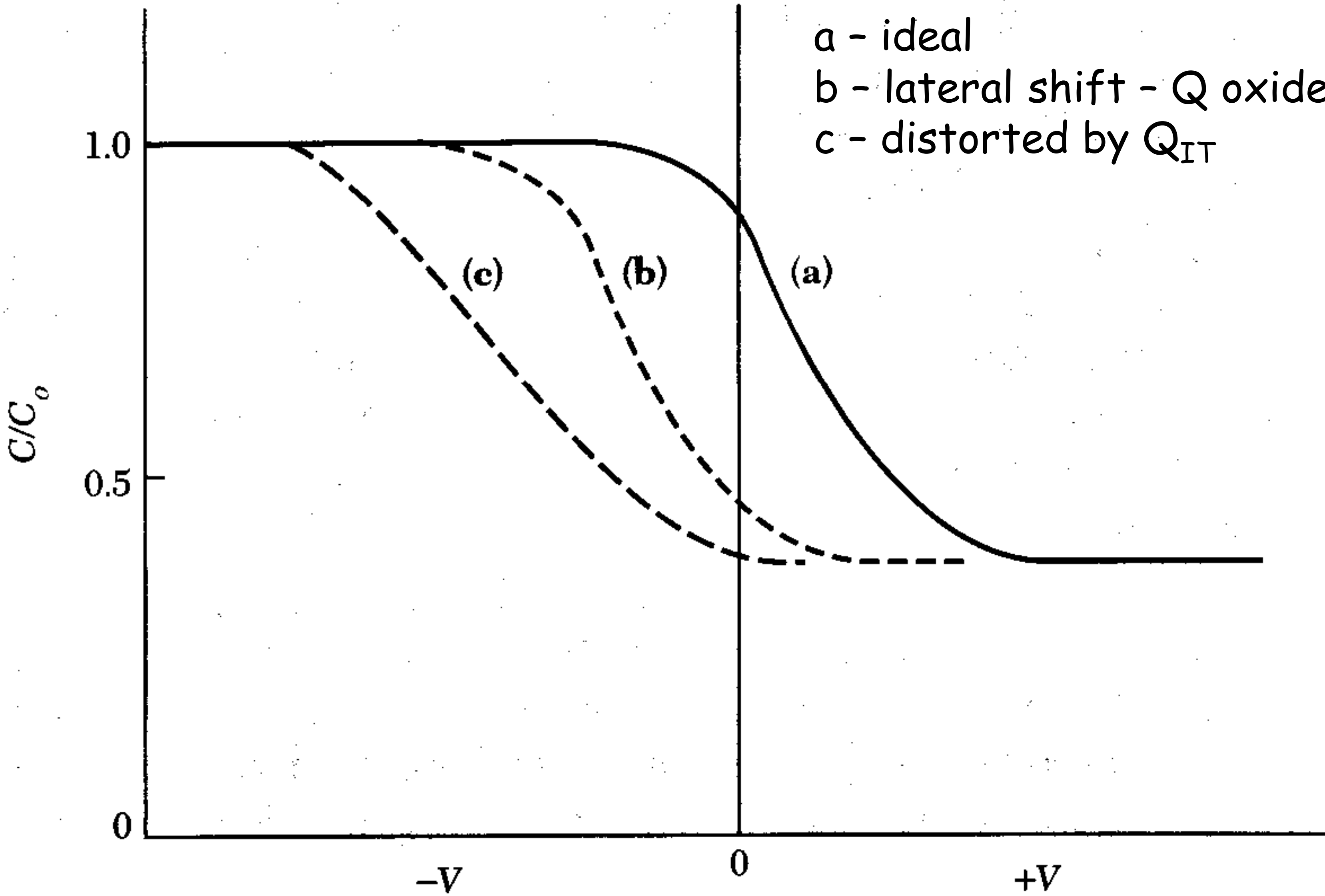
- Surface states – R-G centers caused by disruption of lattice periodicity at surface
- Trap levels distributed in band gap, with Fermi-type distributed:

$$\frac{N_D^+}{N_D} = \frac{1}{1 + g_D e^{-(E_F - E_D)/kT}}$$

- Ionization and polarity will depend on applied voltage (above or below Fermi level
- Frequency dependent capacitance due to surface recombination lifetime compared with measurement frequency
- Effect is to distort CV curve depending on frequency
- Can be passivated w/H anneal – $10^{10}/cm^2$ in Si/SiO_2 system

Effect of Interface trapped charge on C-V curve





a – ideal
b – lateral shift – Q oxide, ϕ_{ms}
c – distorted by Q_{IT}

Non-Ideal MOS capacitor C-V curves

- Work function difference and oxide charges shift CV curve in voltage from ideal case
- CV shift changes threshold voltage
- Mobile ionic charges can change threshold voltage as a function of time – reliability problems
- Interface Trapped Charge distorts CV curve – frequency dependent capacitance
- Interface state density can be reduced by H annealing in Si-SiO_2
- Other gate insulator materials tend to have much higher interface state densities

All of the above….

- For the three types of oxide charges the CV curve is shifted by the voltage on the capacitor Q/C

$$V_{FB-oxide\_charge} = \frac{-1}{C_i}\left[\frac{1}{d}\int_0^d x\rho(x)dx\right]$$

- When work function differences and oxide charges are present, the flat band voltage shift is:

$$V_{FB} = \phi_{ms} - \frac{(Q_f - Q_m - Q_{ot})}{C_i}$$

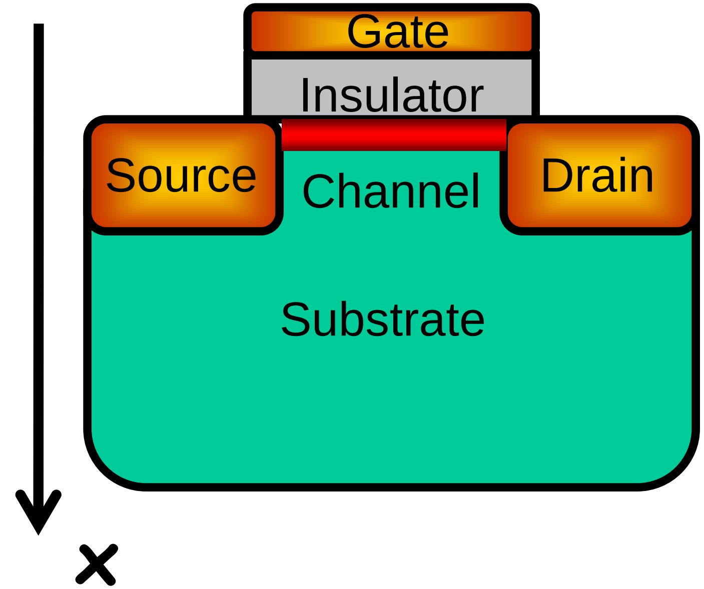
Some important equations in the inversion regime (Depth direction)

$$V_T = \phi_{ms} + 2\psi_B + \psi_{ox}$$

$$\psi_{ox} = Q_s/C_{ox}$$

$$Q_s = qN_A W_{dm}$$

$$W_{dm} = \sqrt{[2\varepsilon_S(2\psi_B)/qN_A]}$$



$$V_T = \phi_{ms} + 2\psi_B + (\sqrt{[4\varepsilon_S\psi_B qN_A]} - Q_f + Q_m + Q_{ot})/C_{ox}$$

$$Q_{inv} = C_{ox}(V_G - V_T)$$