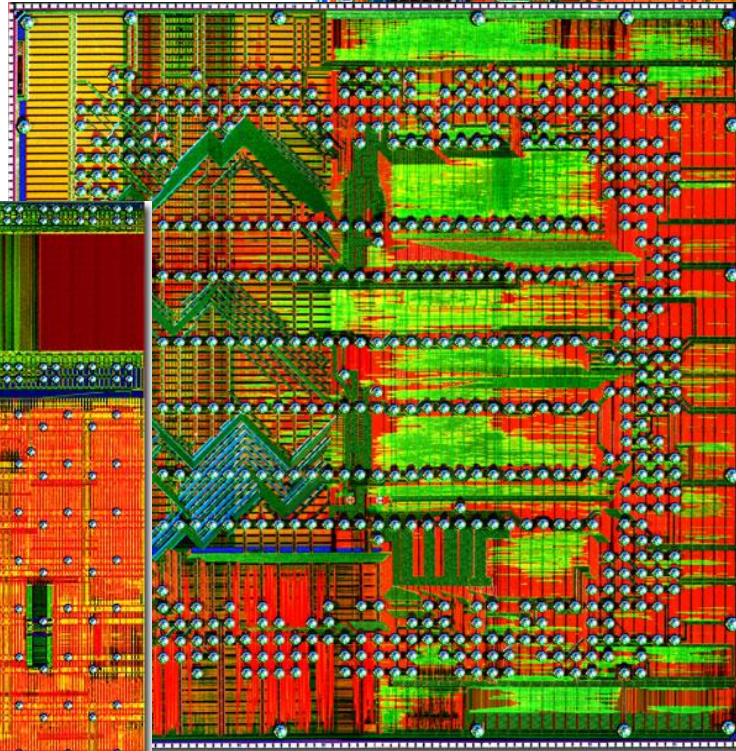
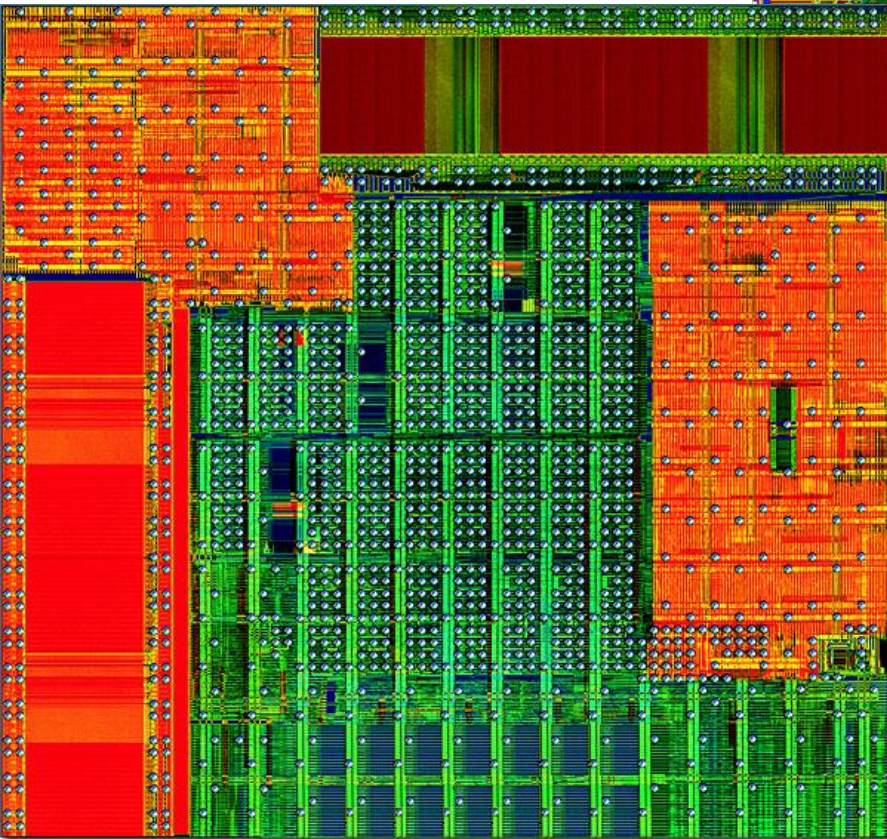
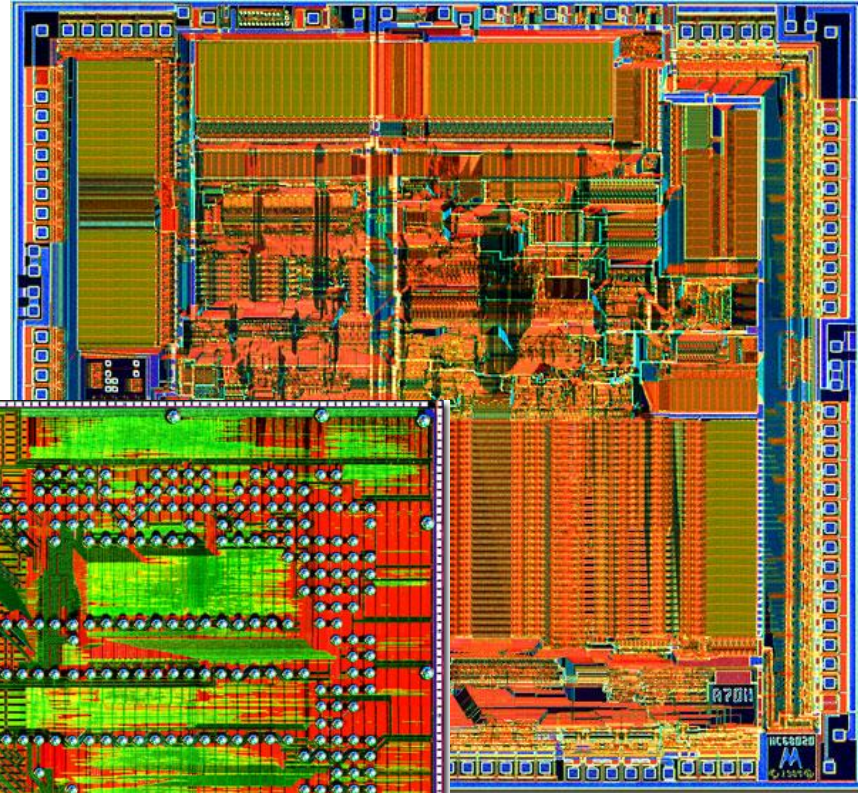


# *Field Effect Transistors*

IBM/Motorola Power PC620



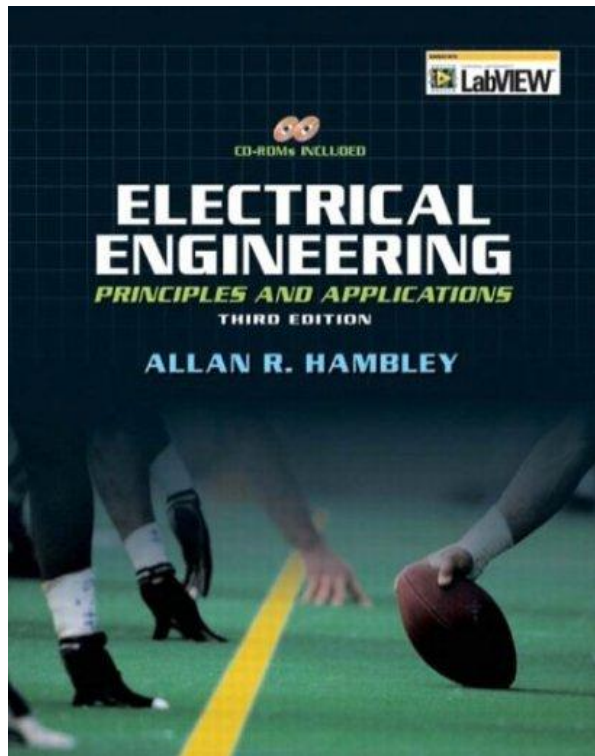
IBM Power PC 601



Motorola MC68020

EE314

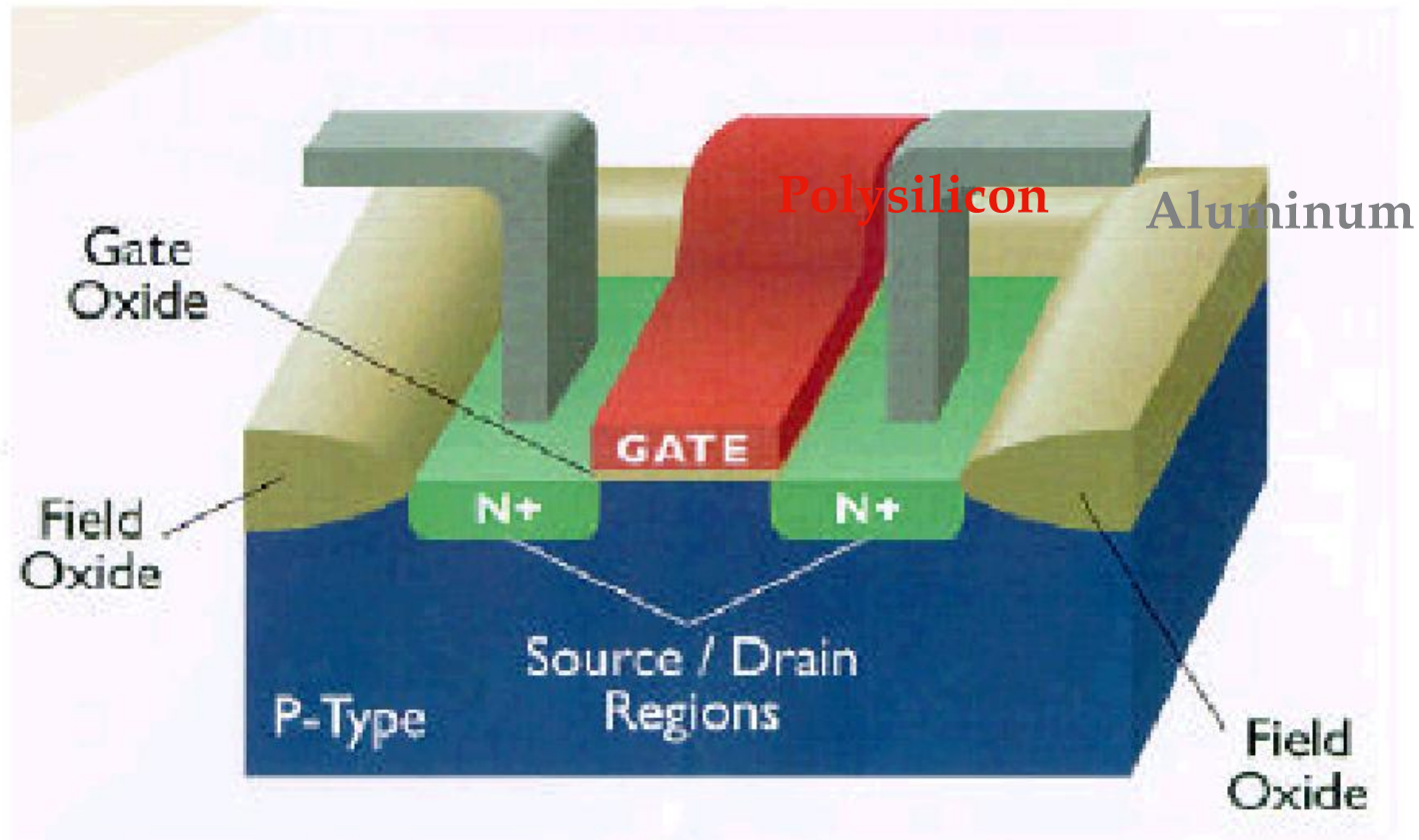




- 1. Construction of MOS*
- 2. NMOS and PMOS*
- 3. Types of MOS*
- 4. MOSFET Basic Operation*
- 5. Characteristics*

Chapter 12: Field  
Effect Transistors

# The MOS Transistor

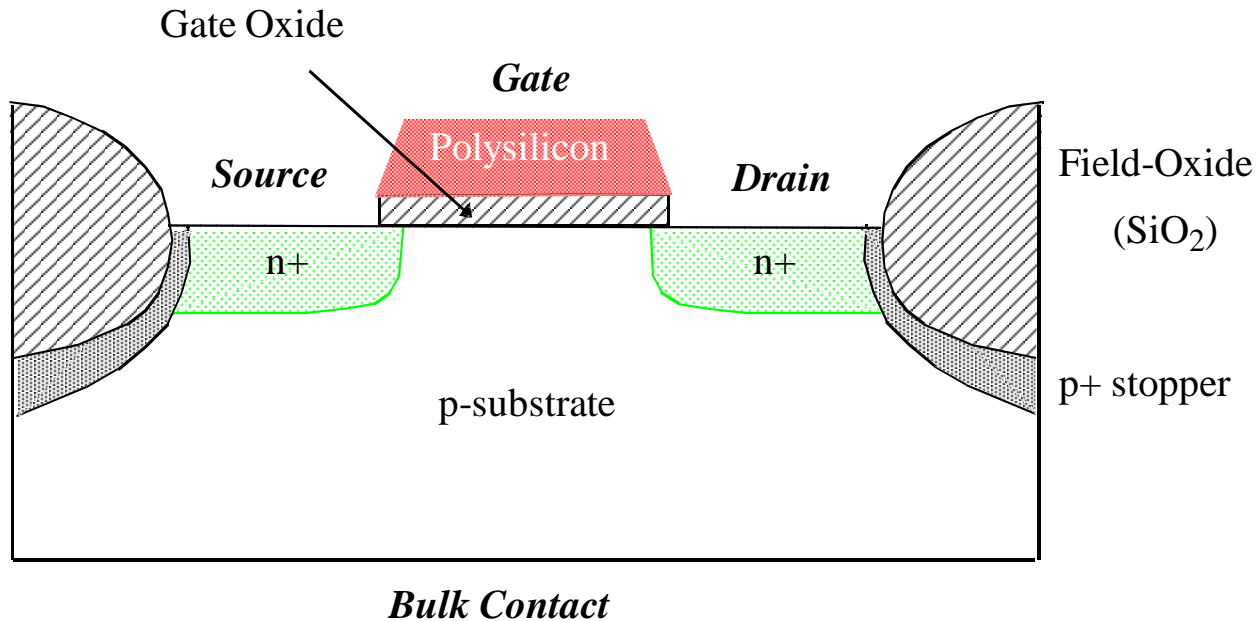


**JFET** - **J**unction **F**ield **E**ffect **T**ransistor

**MOSFET** - **M**etal **O**xide **S**emiconductor Field Effect Transistor

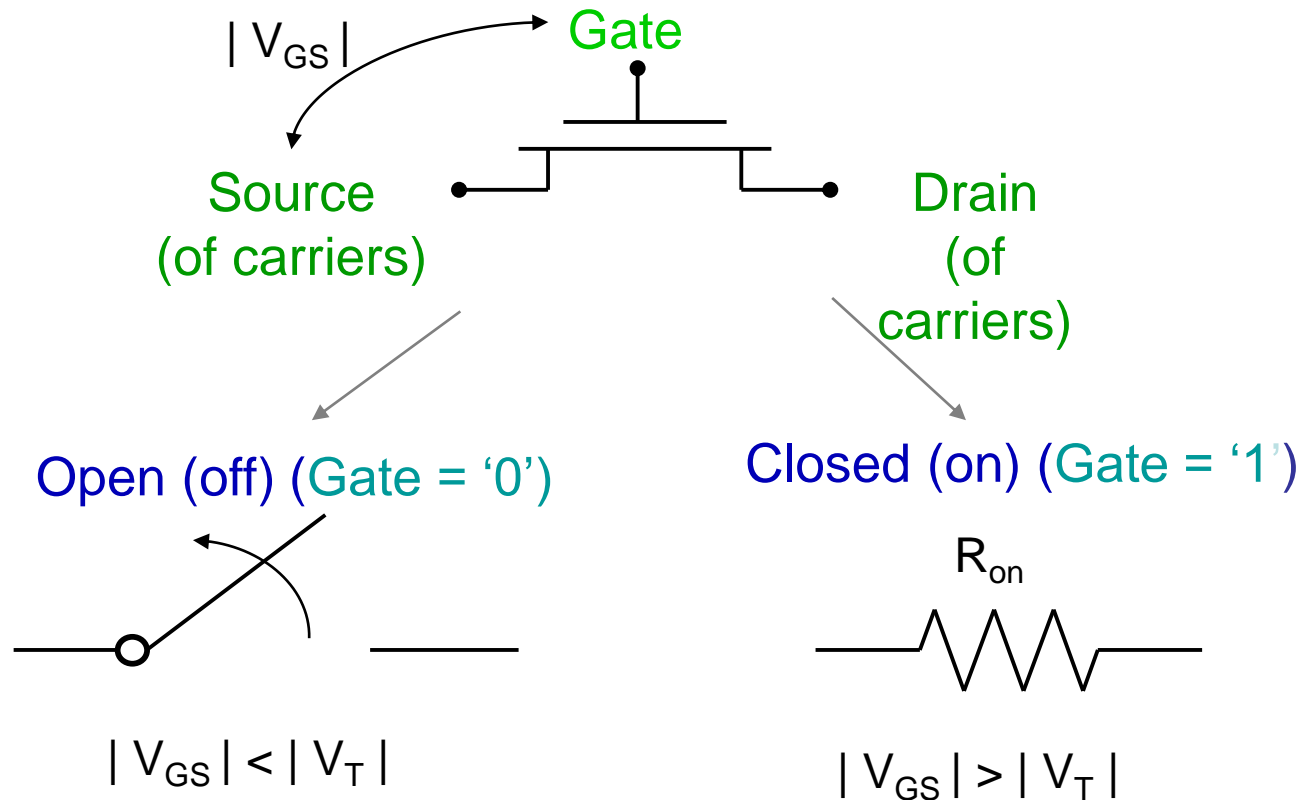
**n-channel MOSFET (nMOS)** & **p-channel MOSFET (pMOS)**

# The MOS Transistor

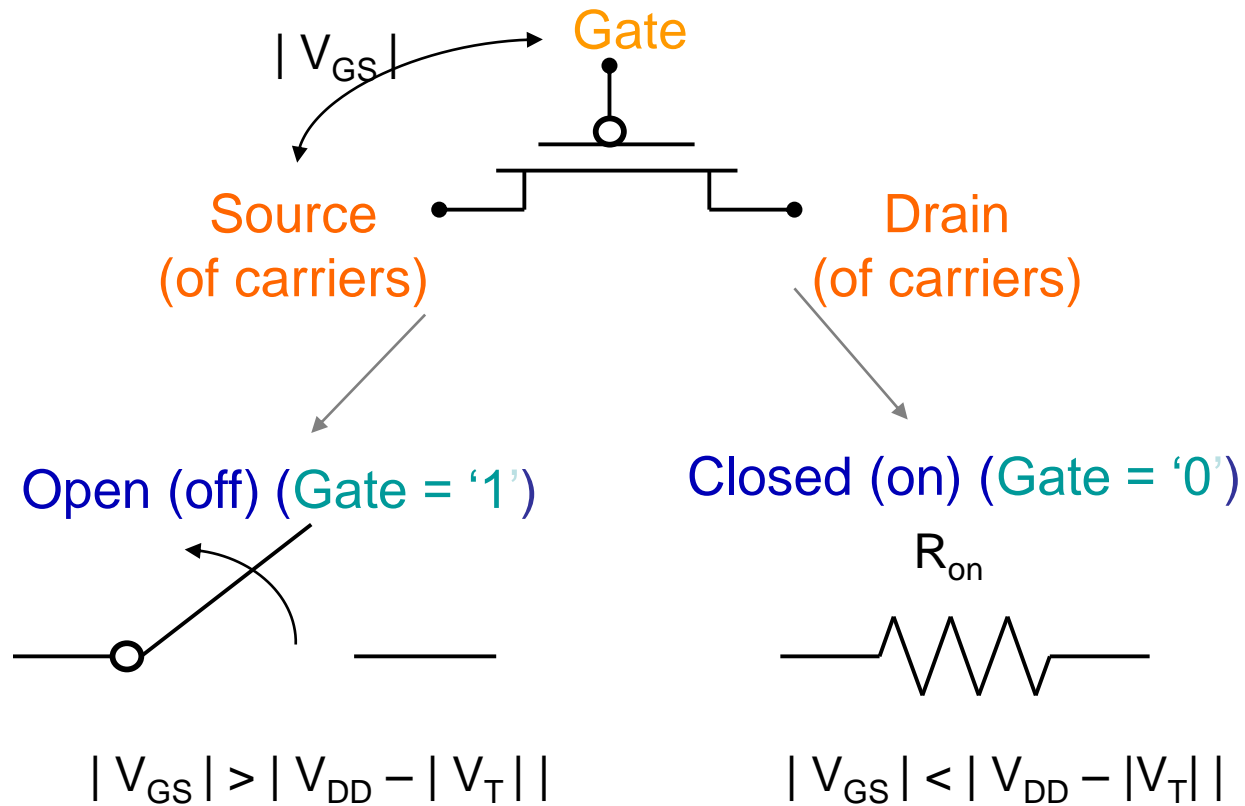


**CROSS-SECTION of NMOS Transistor**

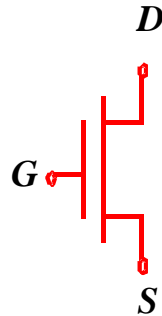
# Switch Model of NMOS Transistor



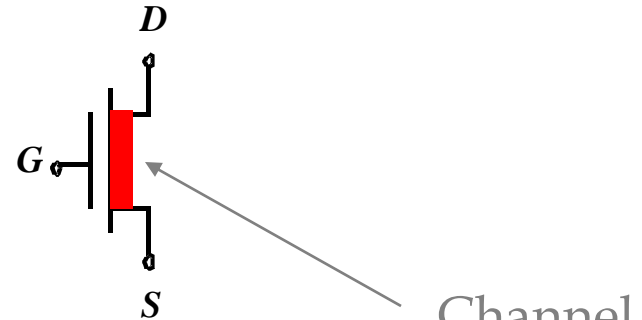
# Switch Model of PMOS Transistor



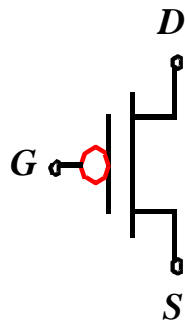
# MOS transistors Symbols



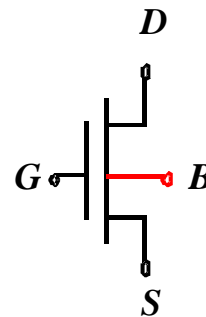
**NMOS Enhancement**



**NMOS Depletion**

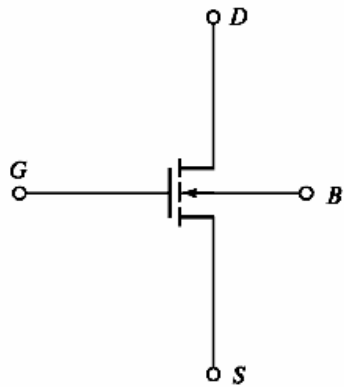


**PMOS Enhancement**

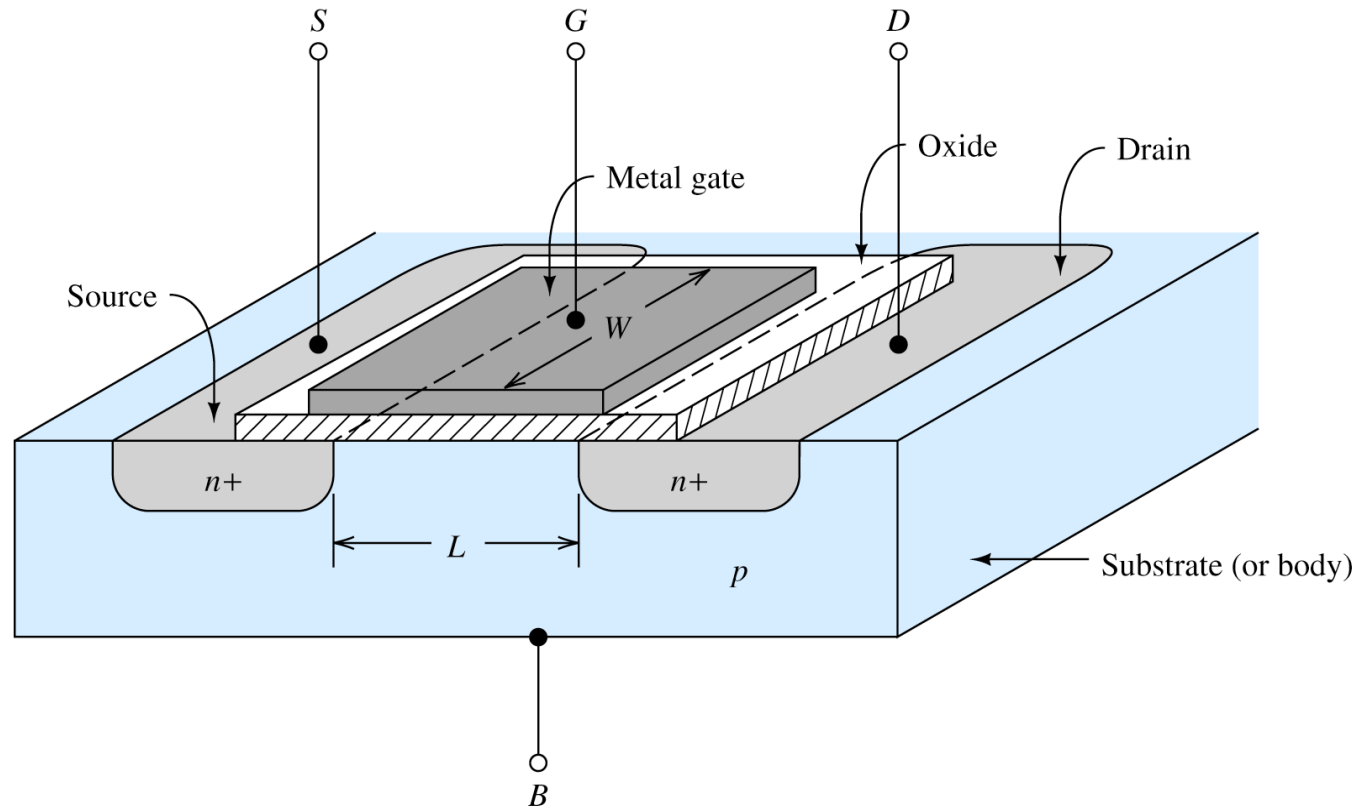


**NMOS with  
Bulk Contact**

# JFET and MOSFET Transistors



Symbol



$L = 0.5-10 \mu\text{m}$

$W = 0.5-500 \mu\text{m}$

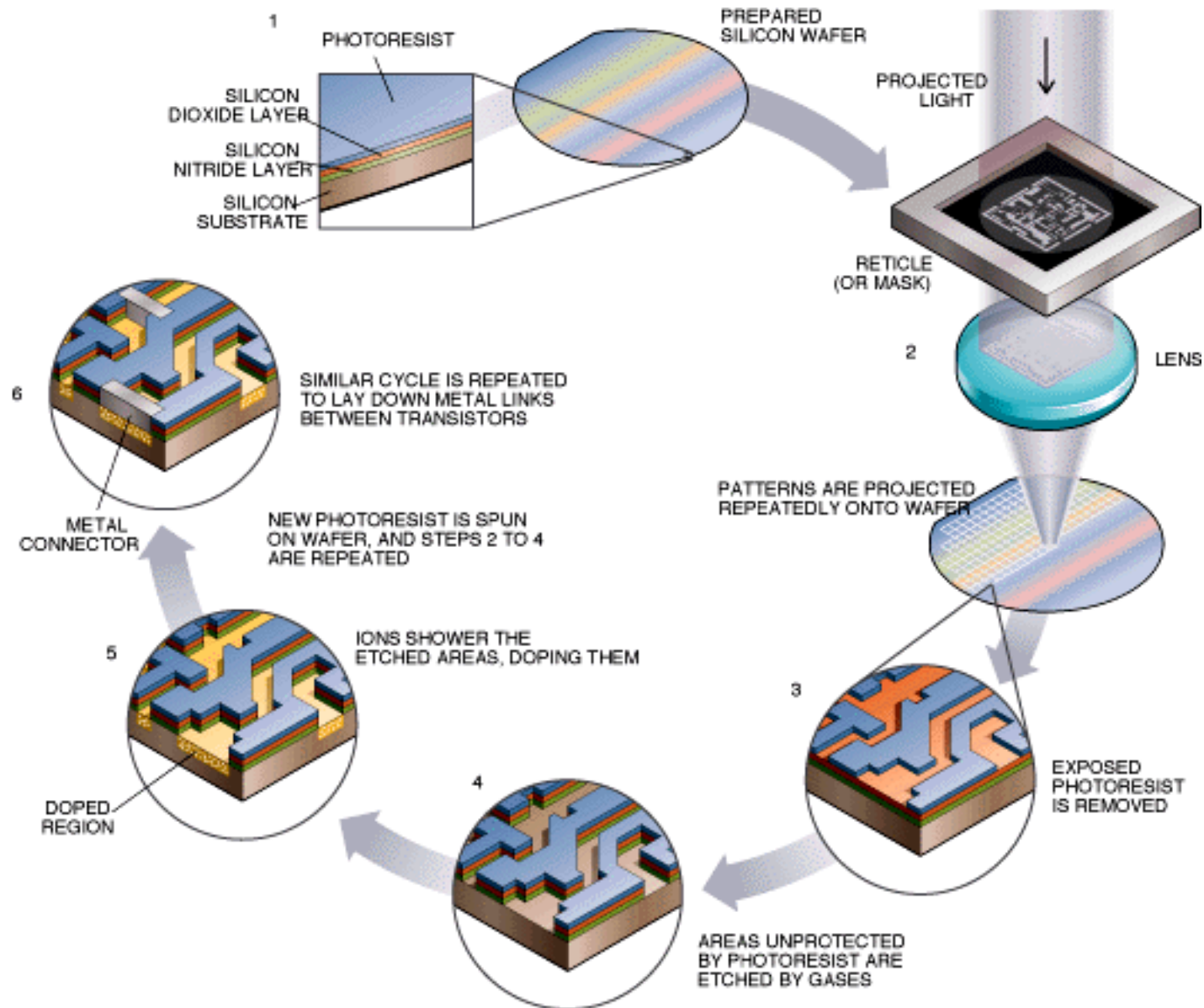
Figure 12.1 *n*-channel enhancement MOSFET showing channel length  $L$  and channel width  $W$ .

$\text{SiO}_2$  Thickness =  $0.02-0.1 \mu\text{m}$

Device characteristics depend on  $L, W$ , Thickness, doping levels



# MOSFET Transistor Fabrication Steps



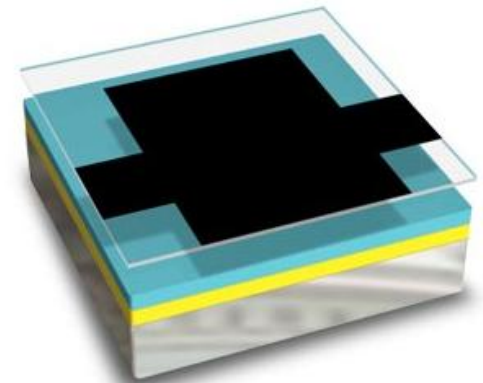
# Building A MOSFET Transistor Using Silicon



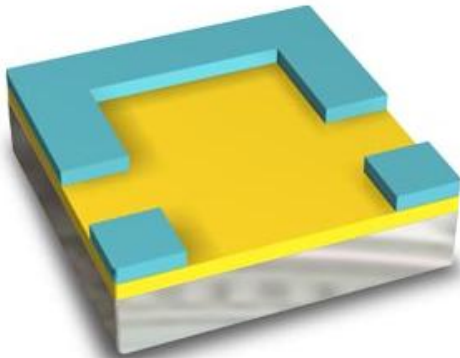
The positively doped silicon wafer is first coated with an insulating layer of silicon dioxide (yellow) through chemical vapor deposition.



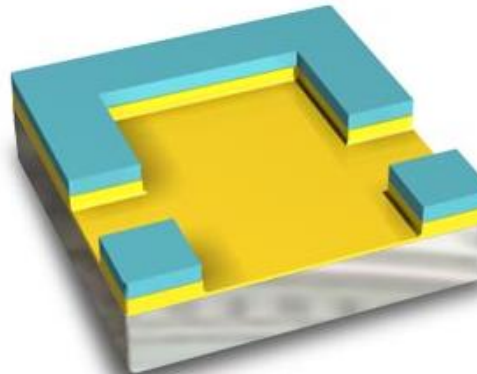
An ultraviolet light-sensitive thin layer of photoresist (blue) is applied to the silicon dioxide surface and evenly spread across the wafer.



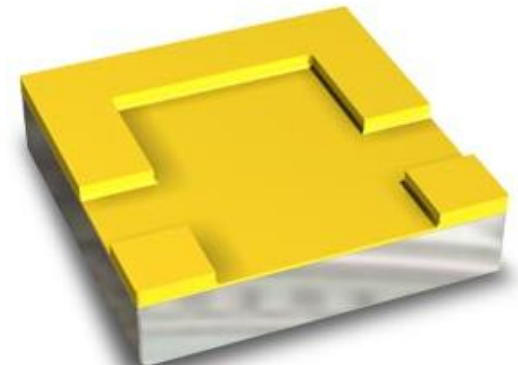
The first mask is placed over the wafer and ultraviolet light is projected onto the mask. Areas of photoresist exposed to the light are hardened and those shielded remain soft.



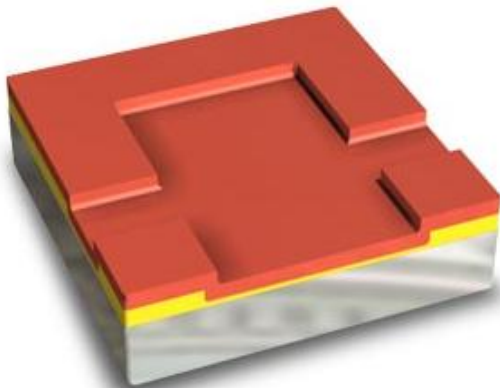
The unexposed (and soft) photoresist is removed by washing with a solvent, leaving the hardened resist and underlying silicon dioxide layer intact.



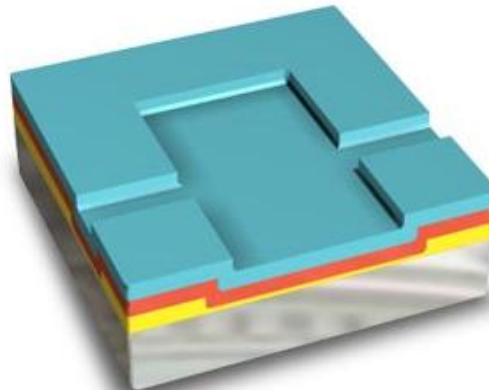
The upper layer of the silicon dioxide is removed by etching with hot gasses, leaving only a very thin layer for insulation.



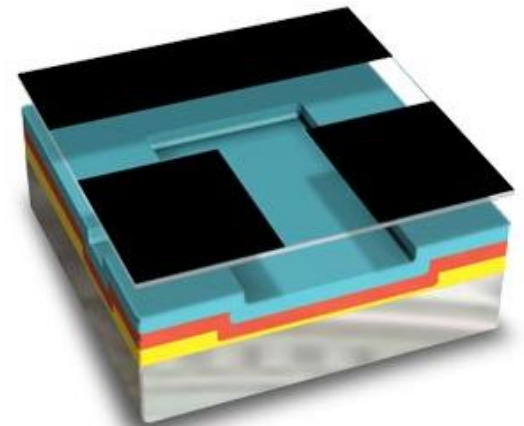
The hardened photoresist is removed with a chemical solvent leaving an uneven silicon dioxide surface over the entire wafer.



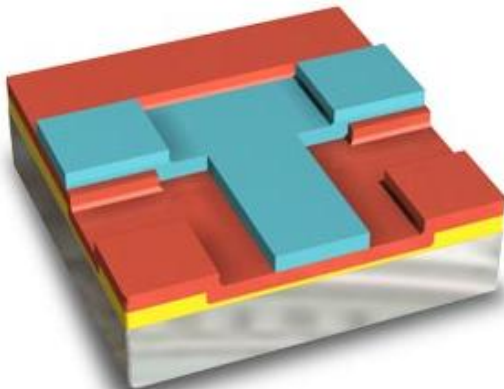
A layer of polysilicon is then deposited onto the silicon dioxide surface using chemical vapor deposition. This material will serve as the transistor's gate.



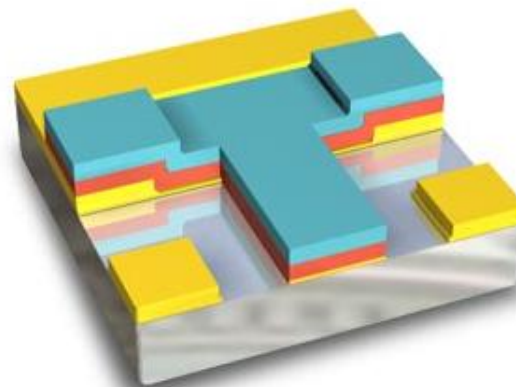
A second layer of photoresist is applied over the polysilicon to prepare the wafer's surface for a second photomask.



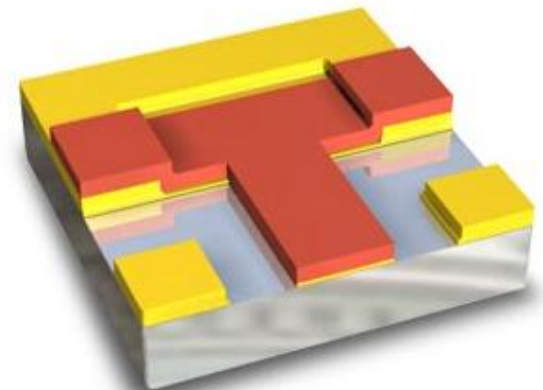
The second mask is placed over the wafer and ultraviolet light is again projected onto the mask. The areas exposed to the light are hardened.



The unexposed photoresist is washed away with a solvent, leaving only the L-shaped hardened resist on the wafer.

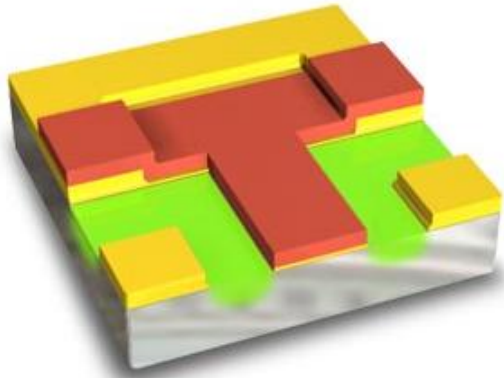


The next step is ion-beam milling (etching) to remove the excess polysilicon and another thin layer of silicon dioxide exposing the silicon wafer's surface.

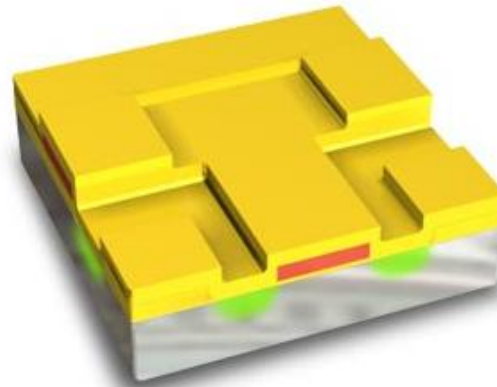


The photoresist is removed with solvent leaving a ridge of polysilicon (the transistor's gate), which rises above the silicon wells.

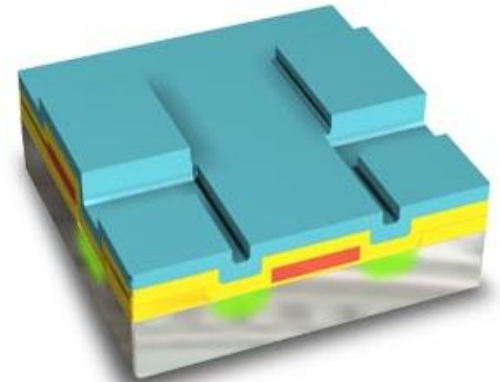




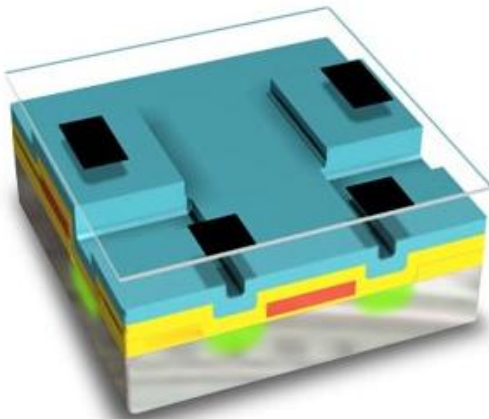
**Chemical doping implants phosphorous (green) deep within the silicon wells surrounded by the silicon dioxide and polysilicon layers to produce positively doped silicon.**



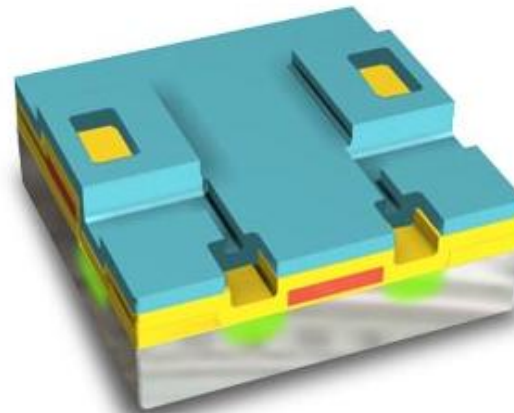
**a second layer of silicon dioxide is applied to provide insulation of the basic transistor structure from metal contacts to be applied later.**



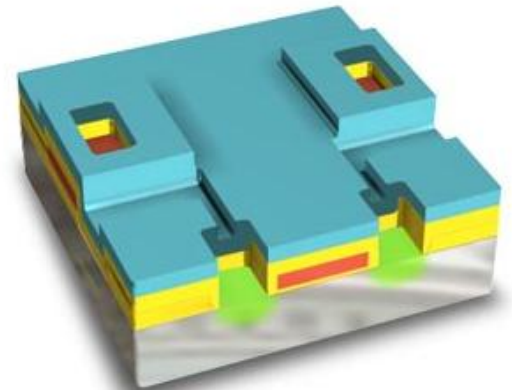
**A third film of photoresist is added to prepare the formation of vertical shafts (vias) that will contain metal contacts for the polysilicon and the wells.**



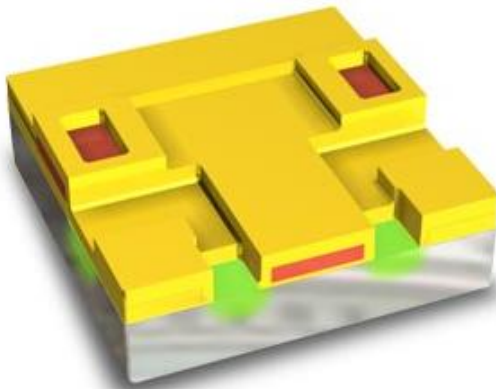
**The third mask is illuminated with ultraviolet light, hardening the photoresist everywhere with the exception of small black rectangles that will become shafts.**



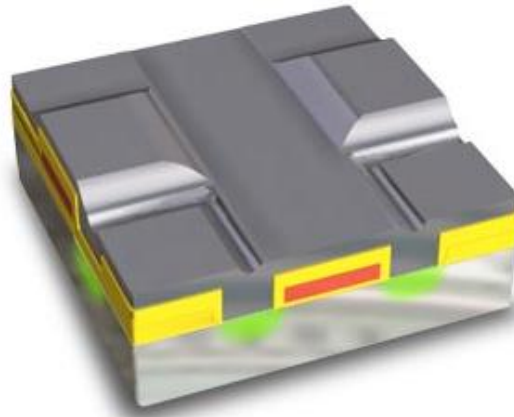
**Removal of the soft photoresist with solvent exposes three areas of exposed silicon dioxide that mark the planned shafts.**



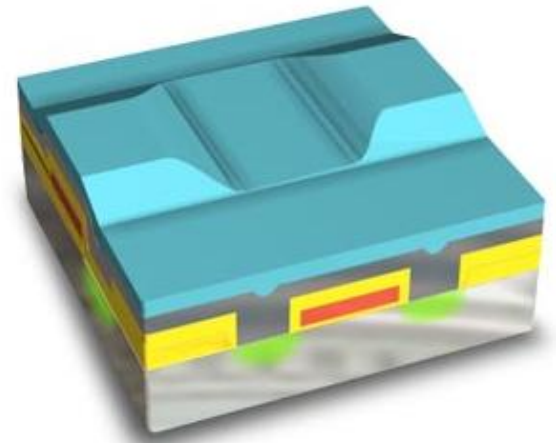
**The wafer is next etched again to remove silicon dioxide and exposing the positively doped silicon and the polysilicon gate.**



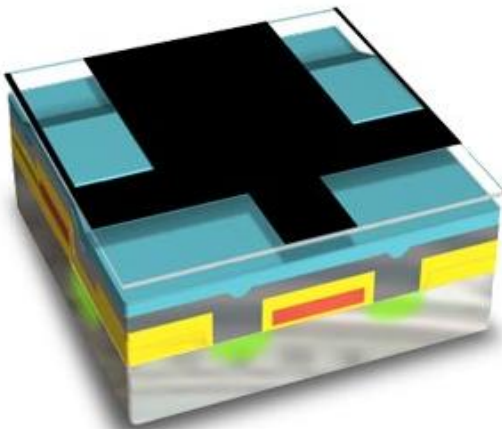
The remaining photoresist is then washed away with solvent. The positively doped silicon areas (green) will serve as the source and the drain.



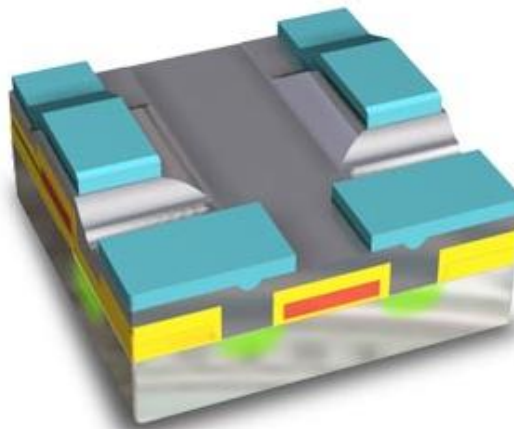
The wafer is then sputter-coated with aluminum that fills the shafts and evenly coats the wafer's surface to provide electrical contacts.



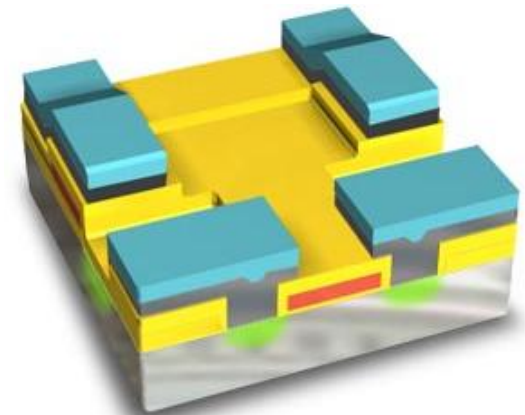
A fourth layer of photoresist is applied to the wafer to prepare the transistor for its final mask, which will produce the pattern for the aluminum "wiring".



Ultraviolet light shining through the metallization mask hardens the photoresist covering the aluminum, which will carry current to and from the transistor.

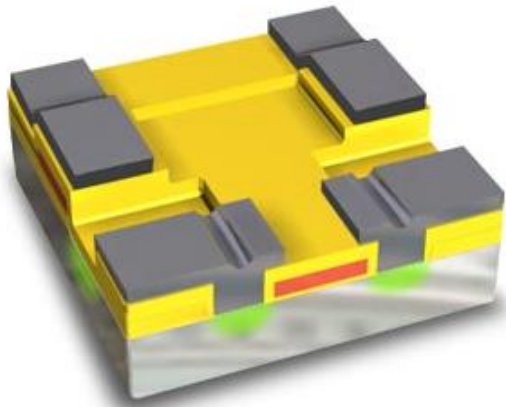


The unexposed photomask is removed with solvent, exposing many bare regions of aluminum that will be removed next.



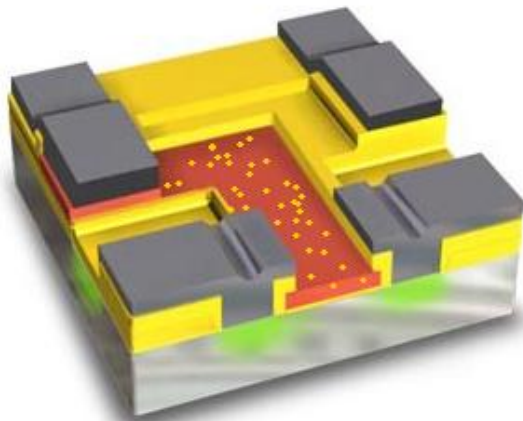
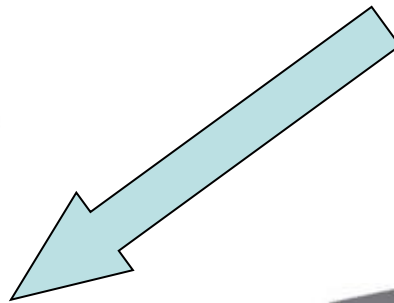
A final etching step removes exposed aluminum leaving only the metal necessary to make contacts in the shafts and connectors on the surface.



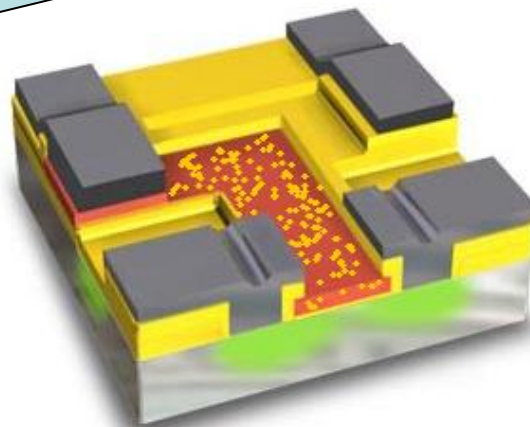


It is done. Now, how does it work?

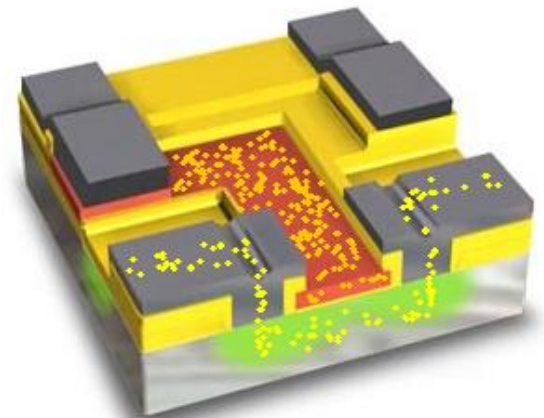
The last resist is washed away with solvent and the transistor is finished, along with millions of its neighbors on the wafer.



Gate Potential  
0.53 V



Gate Potential  
1.96 V



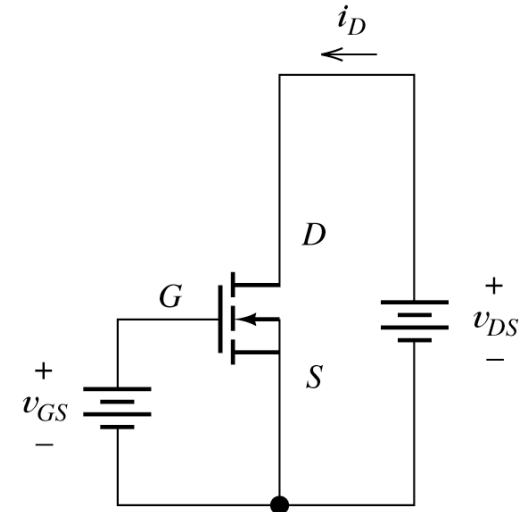
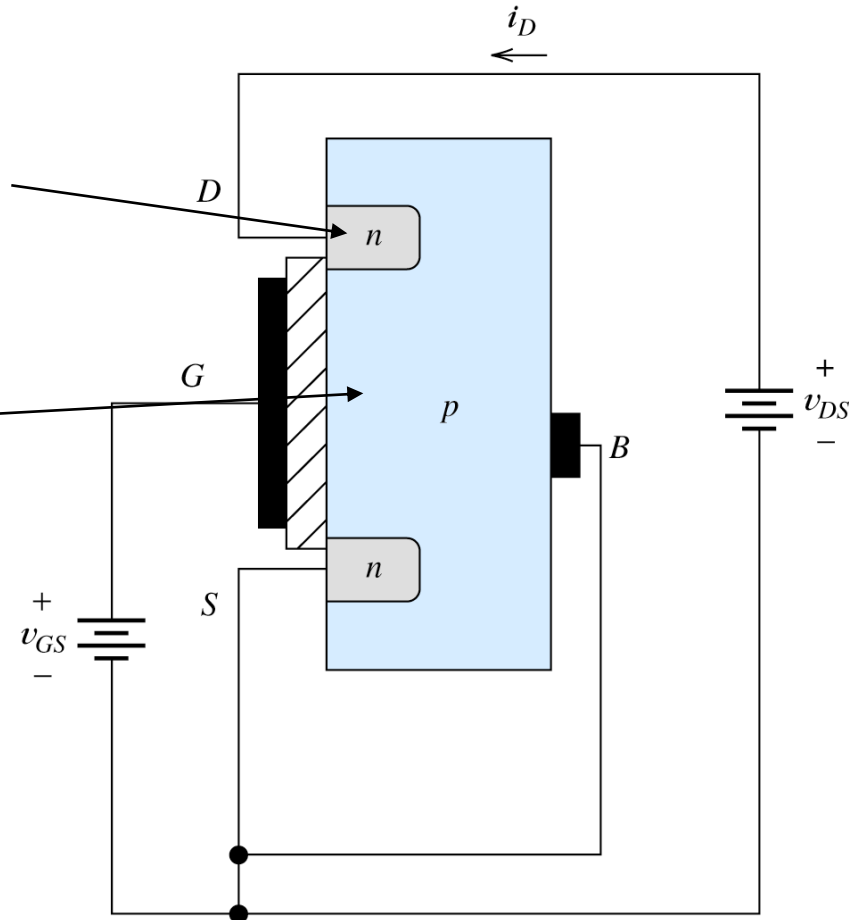
Gate Potential  
2.50 V

# n-channel MOSFET Basic Operation

## Operation in the Cutoff region

pn junction:  
reverse bias

$i_D = 0$   
for  $v_{GS} < V_{t0}$



Schematic

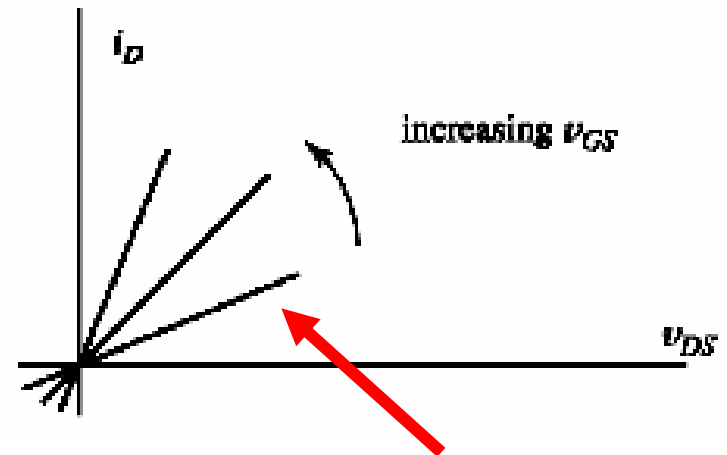
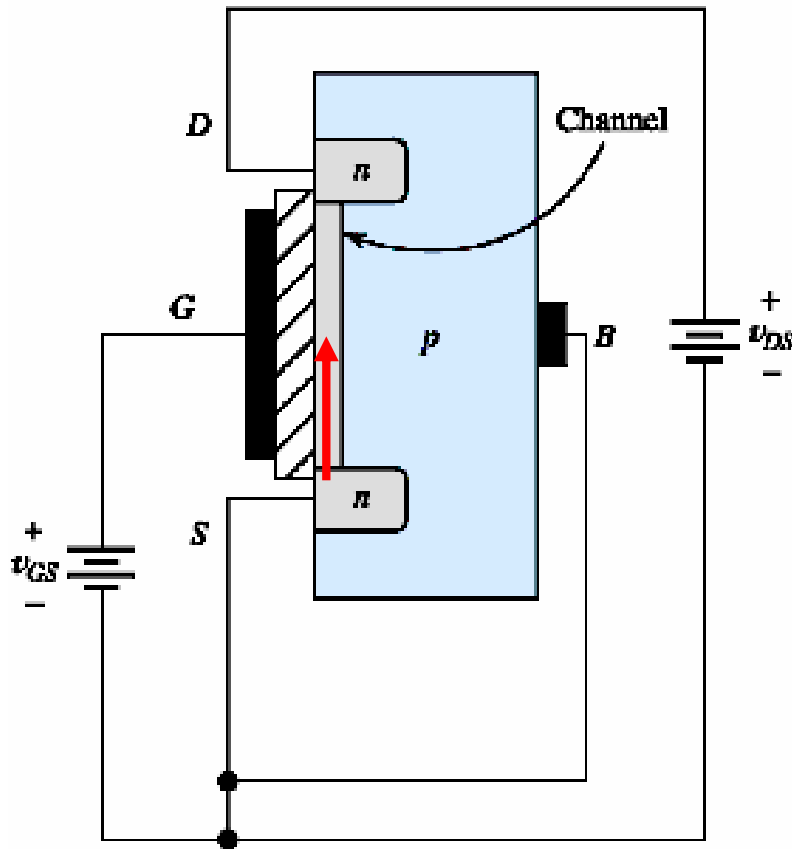
**Figure 12.3** For  $v_{GS} < V_{t0}$ , the  $pn$  junction between drain and body is reverse biased and  $i_D = 0$ .

When  $v_{GS}=0$  then  $i_D=0$  until  $v_{GS} > V_{t0}$  ( $V_{t0}$  -threshold voltage)

# n-channel MOSFET Basic Operation

## Operation in the Triode Region

For  $v_{DS} < v_{GS} - V_{t0}$  and  $v_{GS} > V_{t0}$  the NMOS is operating in the **triode region**

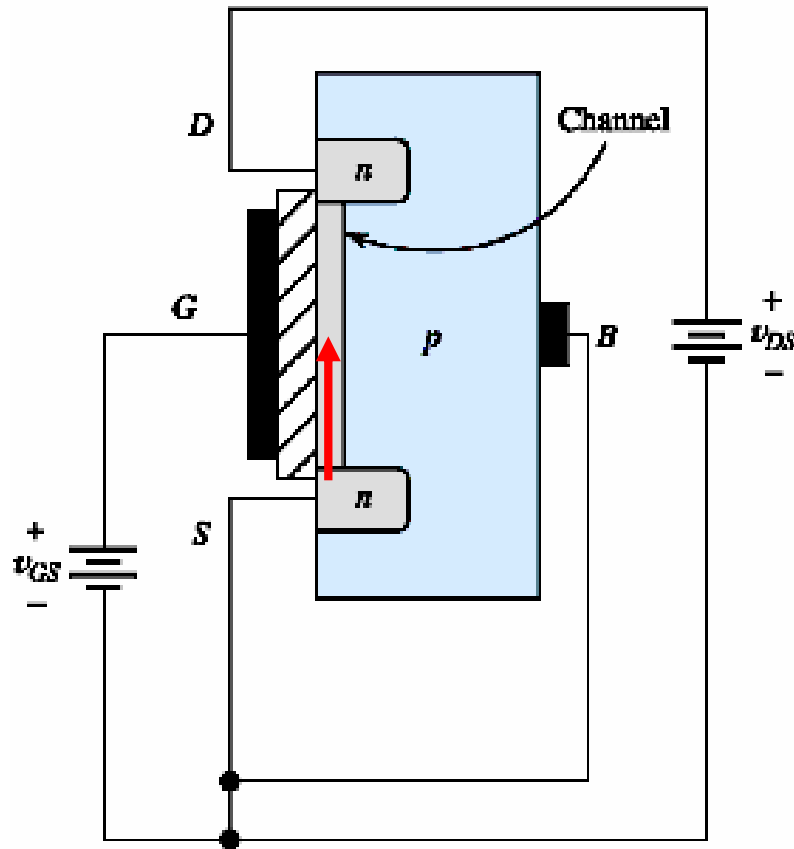


**Resistor like characteristic**  
(R between S & D,  
Used as voltage controlled R)

For small  $v_{DS}$ ,  $i_D$  is proportional  
to the **excess voltage**  $v_{GS} - V_{t0}$

# n-channel MOSFET Basic Operation

## Operation in the Triode Region



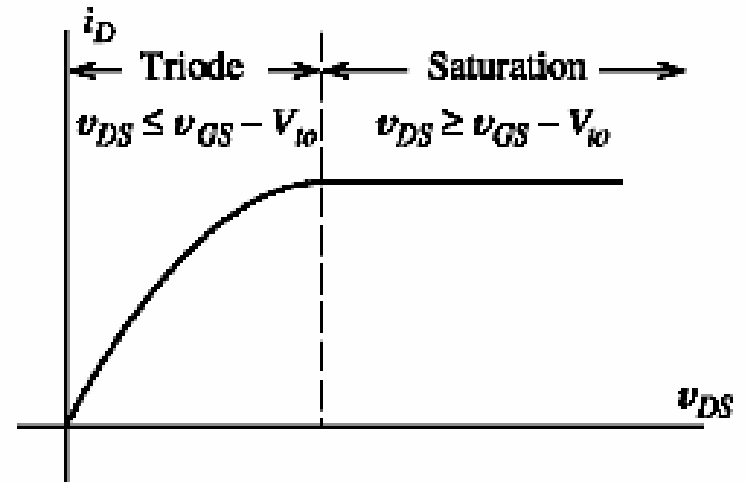
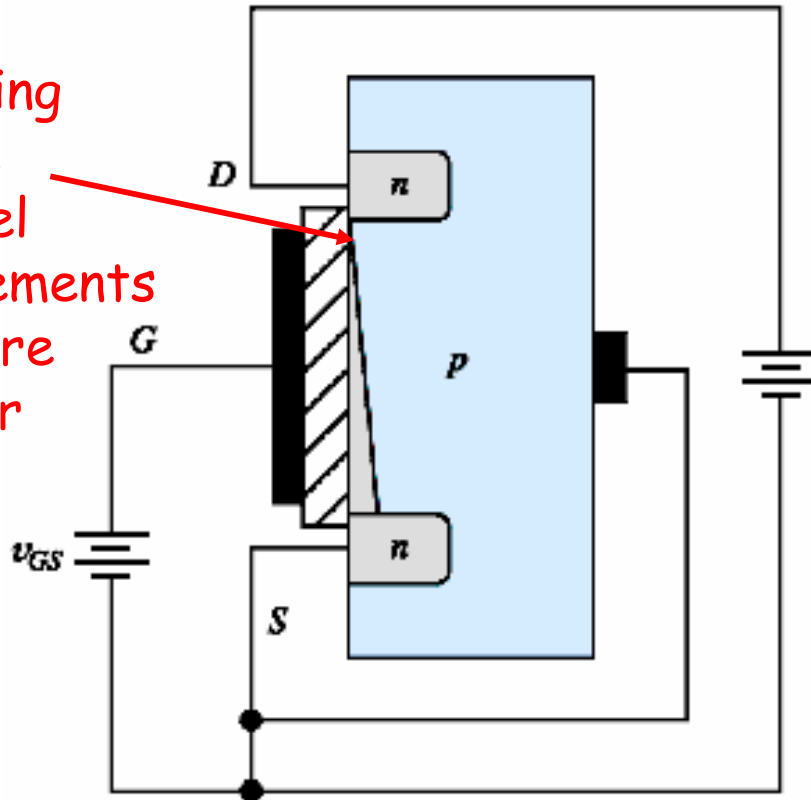
$$i_D = K \left[ 2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2 \right]$$
$$K = \left( \frac{W}{L} \right) \frac{KP}{2}$$

Device parameter KP for NMOSFET is  $50 \mu\text{A}/\text{V}^2$

# n-channel MOSFET Basic Operation

Operation in the Saturation Region ( $v_{DS}$  is increased)

Tapering of the channel - increments of  $i_D$  are smaller when  $v_{DS}$  is larger



When  $v_{GD} = V_{t0}$  then the channel thickness is 0 and

$$i_D = K(v_{GS} - V_{t0})^2$$



# n-channel MOSFET Basic Operation

## Example 12.1

An nMOS has  $W=160\text{ }\mu\text{m}$ ,  $L=2\text{ }\mu\text{m}$ ,  $KP=50\text{ }\mu\text{A/V}^2$  and  $V_{t0}=2\text{ V}$ .

Plot the drain current characteristic vs drain to source voltage for  $v_{GS}=3\text{ V}$ .

$$i_D = K \left[ 2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2 \right]$$

$$i_D = K(v_{GS} - V_{t0})^2$$

$$K = \left( \frac{W}{L} \right) \frac{KP}{2}$$

# n-channel MOSFET Basic Operation

## Example 12.1

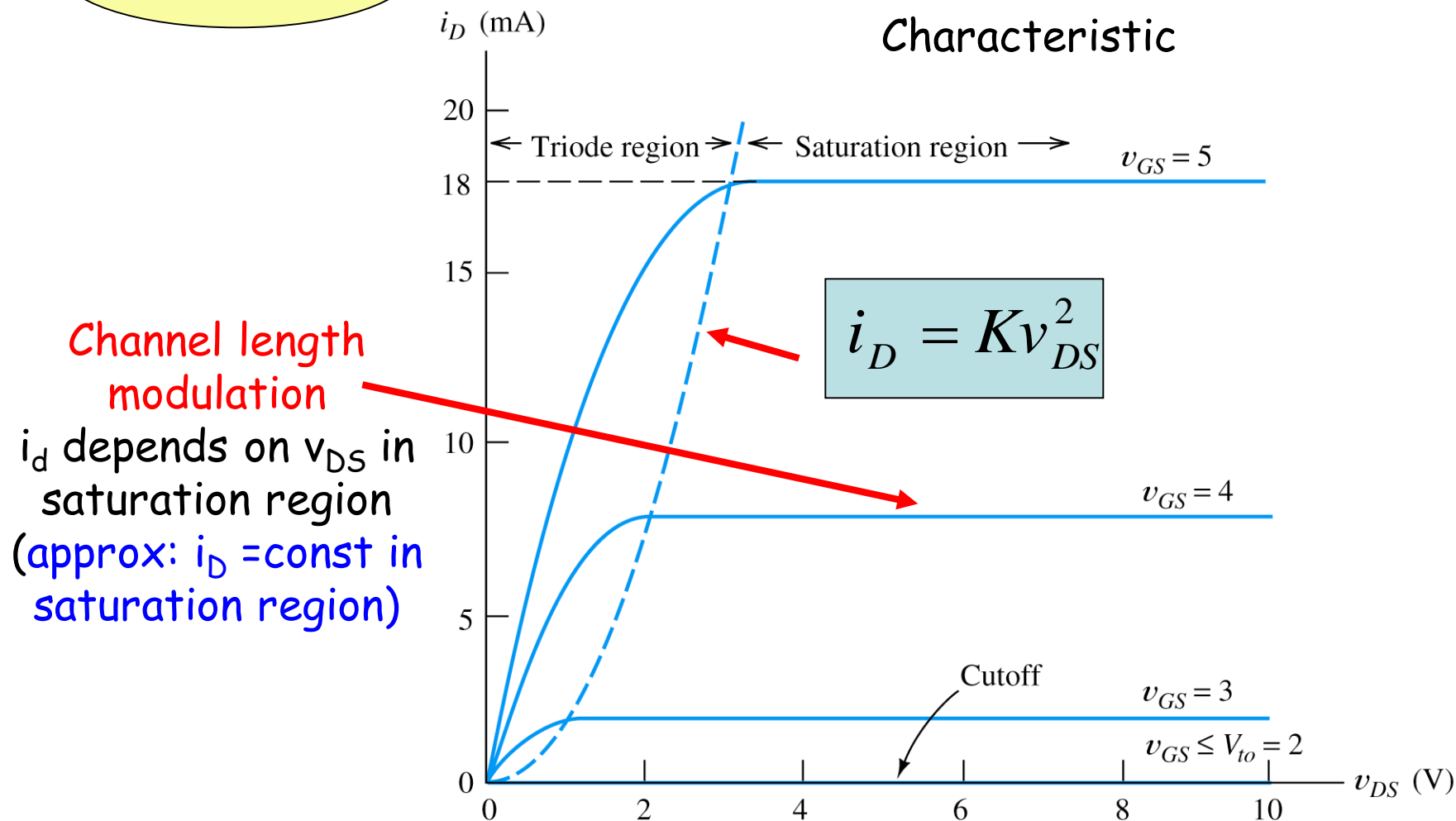


Figure 12.6 Characteristic curves for an NMOS transistor.

# p-channel MOSFET Basic Operation

It is constructed by interchanging the  $n$  and  $p$  regions of n-channel MOSFET.

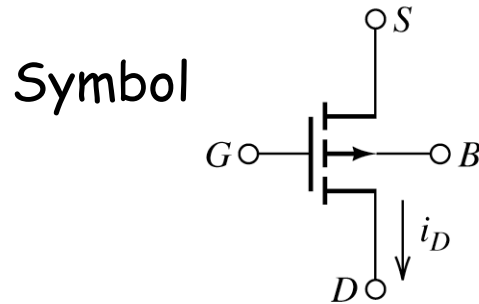


Figure 12.8 Circuit symbol for PMOS transistor.

How does p-channel MOSFET operate?

- voltage polarities
- $-i_D$  current
- schematic

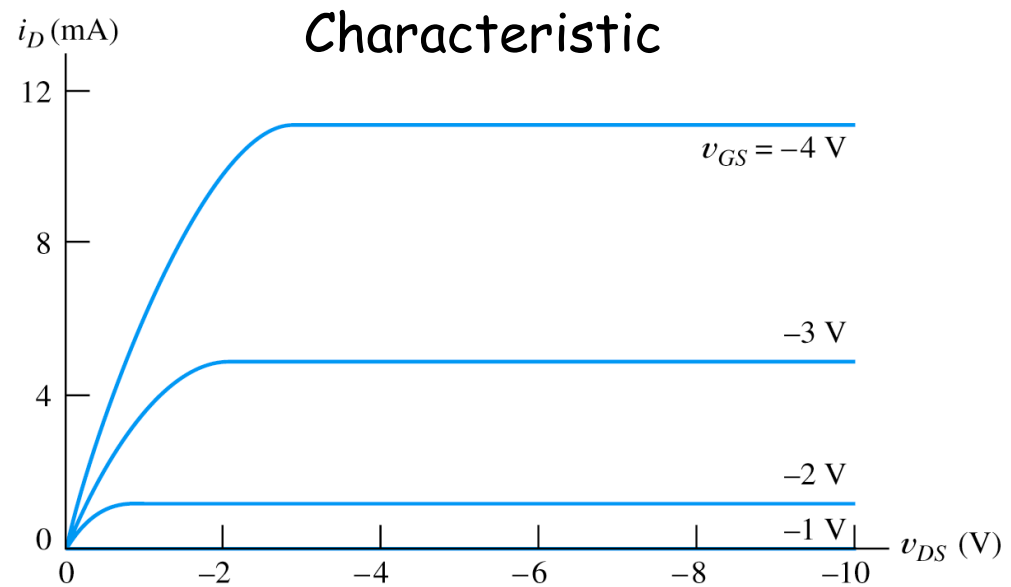


Figure 12.9 Answer for Exercise 12.3.