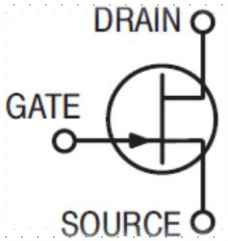
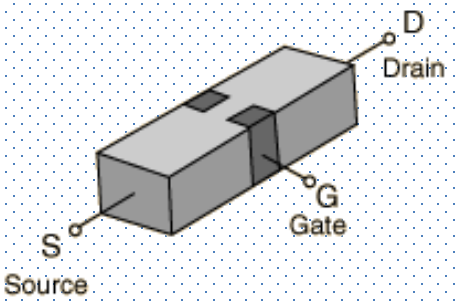


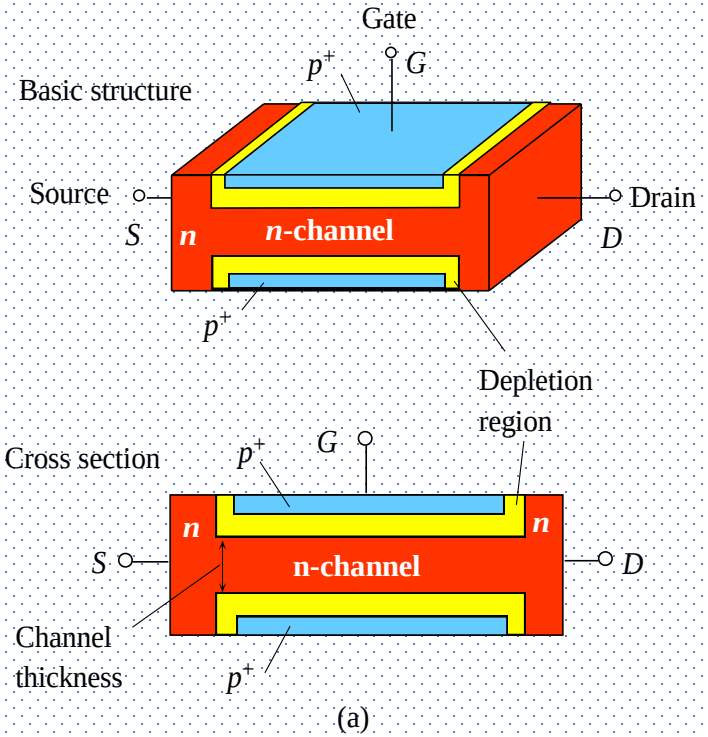


FET

Field Effect Transistors

ELEKTRONIKA KONTROL

Eka Maulana, ST, MT, M.Eng.
Universitas Brawijaya



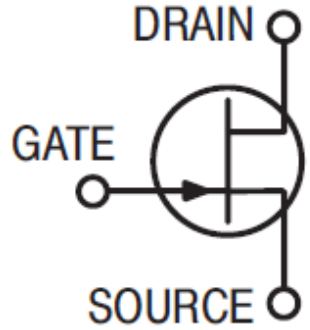
INTRODUCTION TO FET

- FET: FIELD EFFECT TRANSISTOR
- THERE ARE TWO TYPES
  - JFET: JUNCTION FET
  - MOSFET: METAL-OXIDE-SEMICONDUCTOR FET
- MOSFET IS ALSO CALLED THE INSULATED-GATE FET OR IGFET.
  - QUITE SMALL
  - SIMPLE MANUFACTURING PROCESS
  - LOW POWER CONSUMPTION
  - WIDELY USED IN VLSI CIRCUITS(>800 MILLION ON A SINGLE IC CHIP)

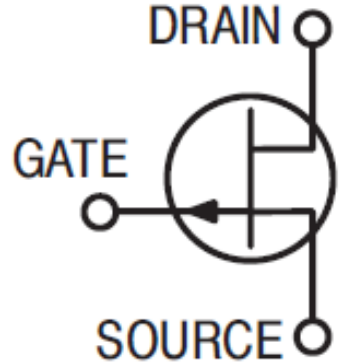
CLASSIFICATION OF FET

- ACCORDING TO THE TYPE OF THE CHANNEL, FETS CAN BE CLASSIFIED AS
  - JFET
    - P CHANNEL
    - N CHANNEL
  - MOSFET
    - N CHANNEL
      - **Enhancement type**
      - **Depletion type**
    - P CHANNEL
      - **Enhancement type**
      - **Depletion type**

SIMBOL JFET DAN MOSFET

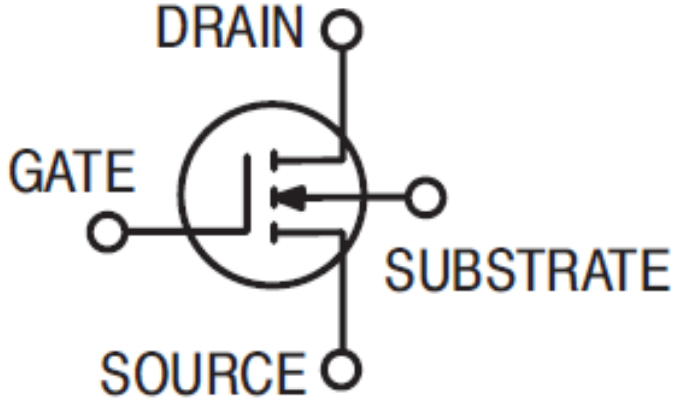


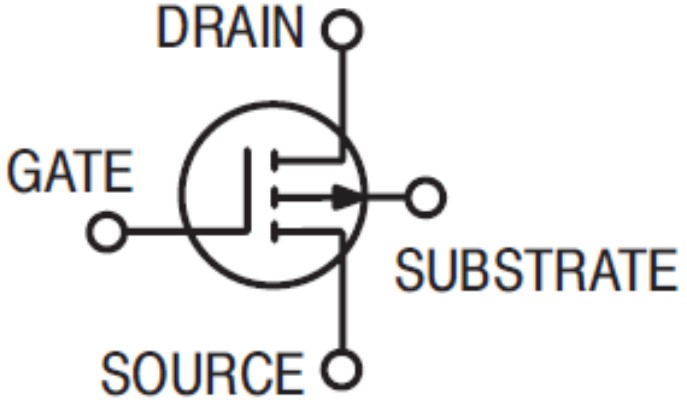
N-CHANNEL JFET



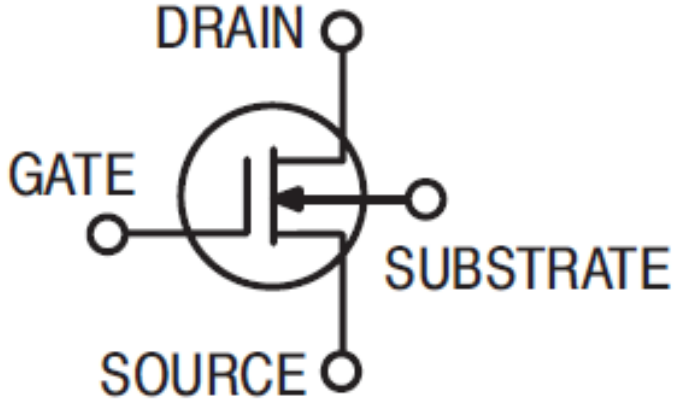
P-CHANNEL JFET

TYPE C

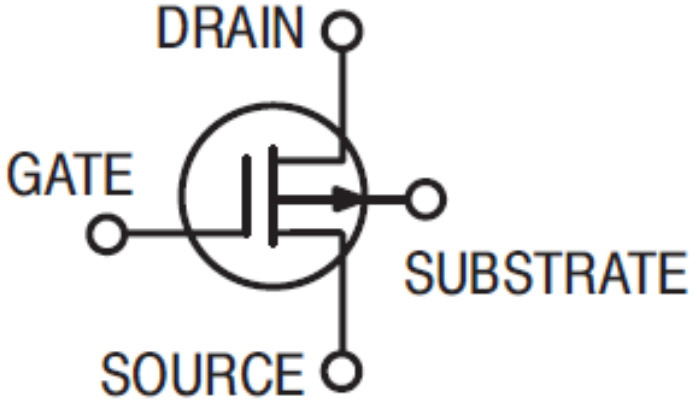




TYPE B



N-CHANNEL MOSFET



P-CHANNEL MOSFET

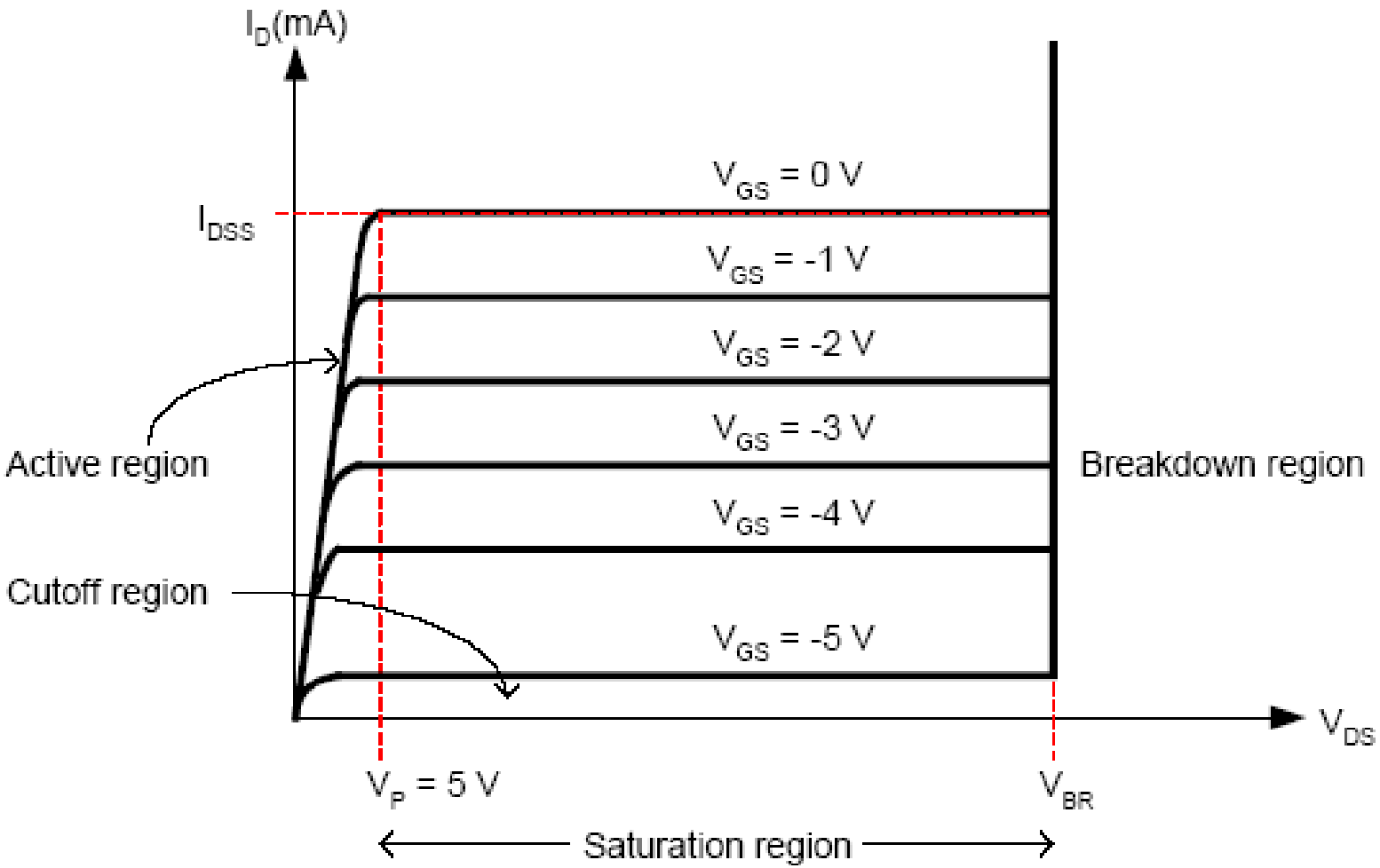
THE FIELD EFFECT TRANSISTOR (FET)

- IN 1945, SHOCKLEY HAD AN IDEA FOR MAKING A SOLID STATE DEVICE OUT OF SEMICONDUCTORS.
- HE REASONED THAT A STRONG ELECTRICAL FIELD COULD CAUSE THE FLOW OF ELECTRICITY WITHIN A NEARBY SEMICONDUCTOR.
- HE TRIED TO BUILD ONE, BUT IT DIDN'T WORK.
- THREE YEARS LATER, BRATTAIN & BARDEEN BUILT THE FIRST WORKING TRANSISTOR, THE GERMANIUM POINT-CONTACT TRANSISTOR, WHICH WAS DESIGNED AS THE JUNCTION (SANDWICH) TRANSISTOR.
- IN 1960 BELL SCIENTIST JOHN ATALLA DEVELOPED A NEW DESIGN BASED ON SHOCKLEY'S ORIGINAL FIELD-EFFECT THEORIES.
- BY THE LATE 1960S, MANUFACTURERS CONVERTED FROM JUNCTION TYPE INTEGRATED CIRCUITS TO FIELD EFFECT DEVICES.

THE FIELD EFFECT TRANSISTOR (FET)

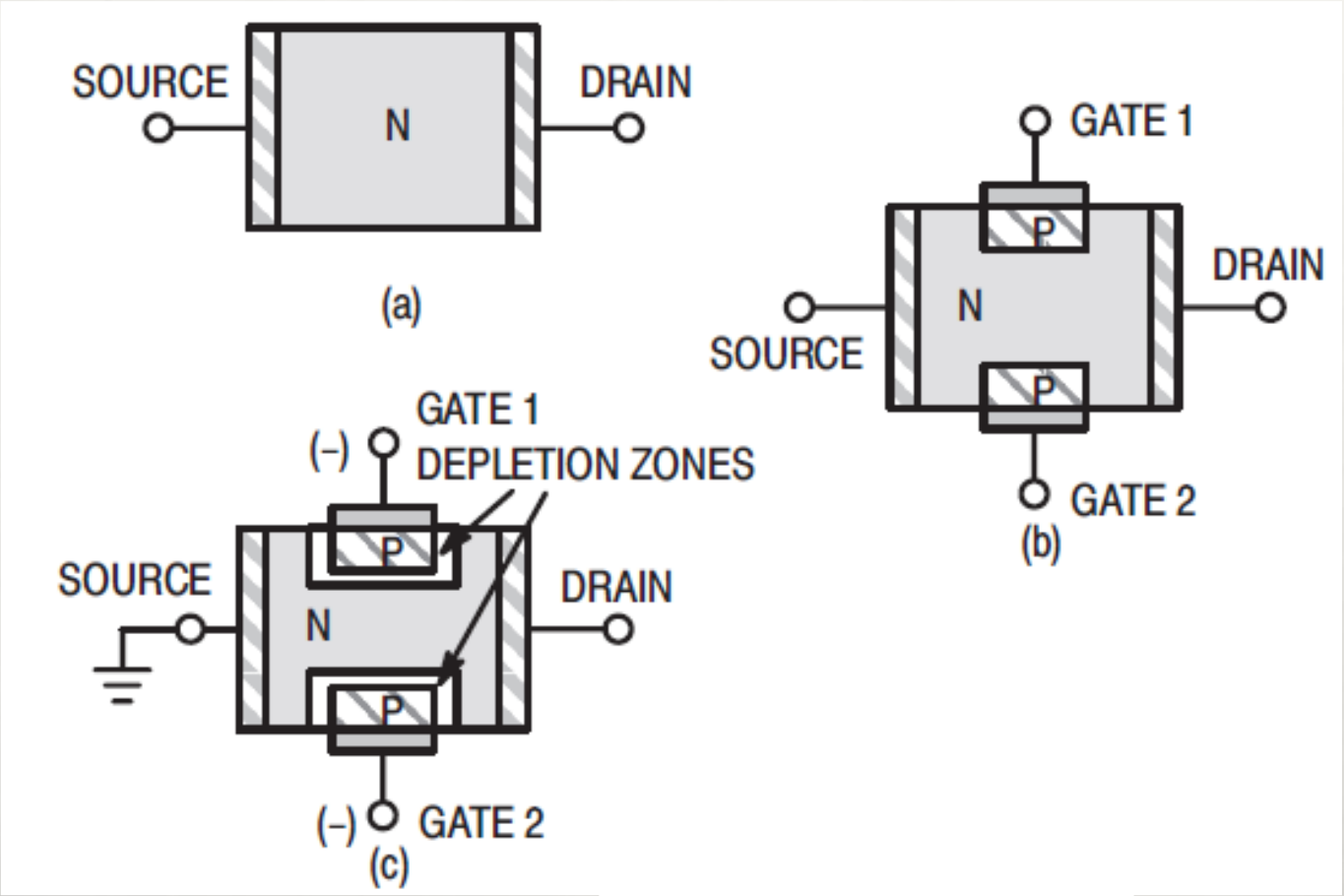
- FIELD EFFECT DEVICES ARE THOSE IN WHICH CURRENT IS CONTROLLED BY THE ACTION OF AN ELECTRON FIELD, RATHER THAN CARRIER INJECTION.
- FIELD-EFFECT TRANSISTORS ARE SO NAMED BECAUSE A WEAK ELECTRICAL SIGNAL COMING IN THROUGH ONE ELECTRODE CREATES AN ELECTRICAL FIELD THROUGH THE REST OF THE TRANSISTOR.
- THE FET WAS KNOWN AS A "UNIPOLAR" TRANSISTOR.
- THE TERM REFERS TO THE FACT THAT CURRENT IS TRANSPORTED BY CARRIERS OF ONE POLARITY (MAJORITY), WHEREAS IN THE CONVENTIONAL BIPOLAR TRANSISTOR CARRIERS OF BOTH POLARITIES (MAJORITY AND MINORITY) ARE INVOLVED.

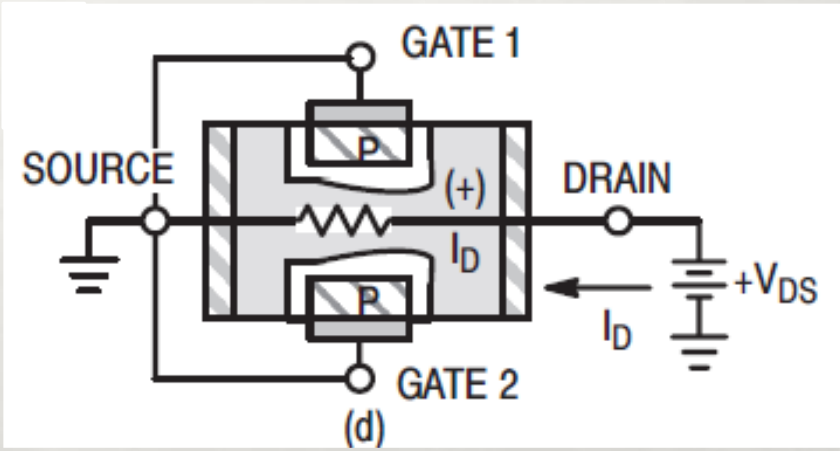
- The relationship between V_{GS}, V_{DS} and I_{DSS} is as shown below.



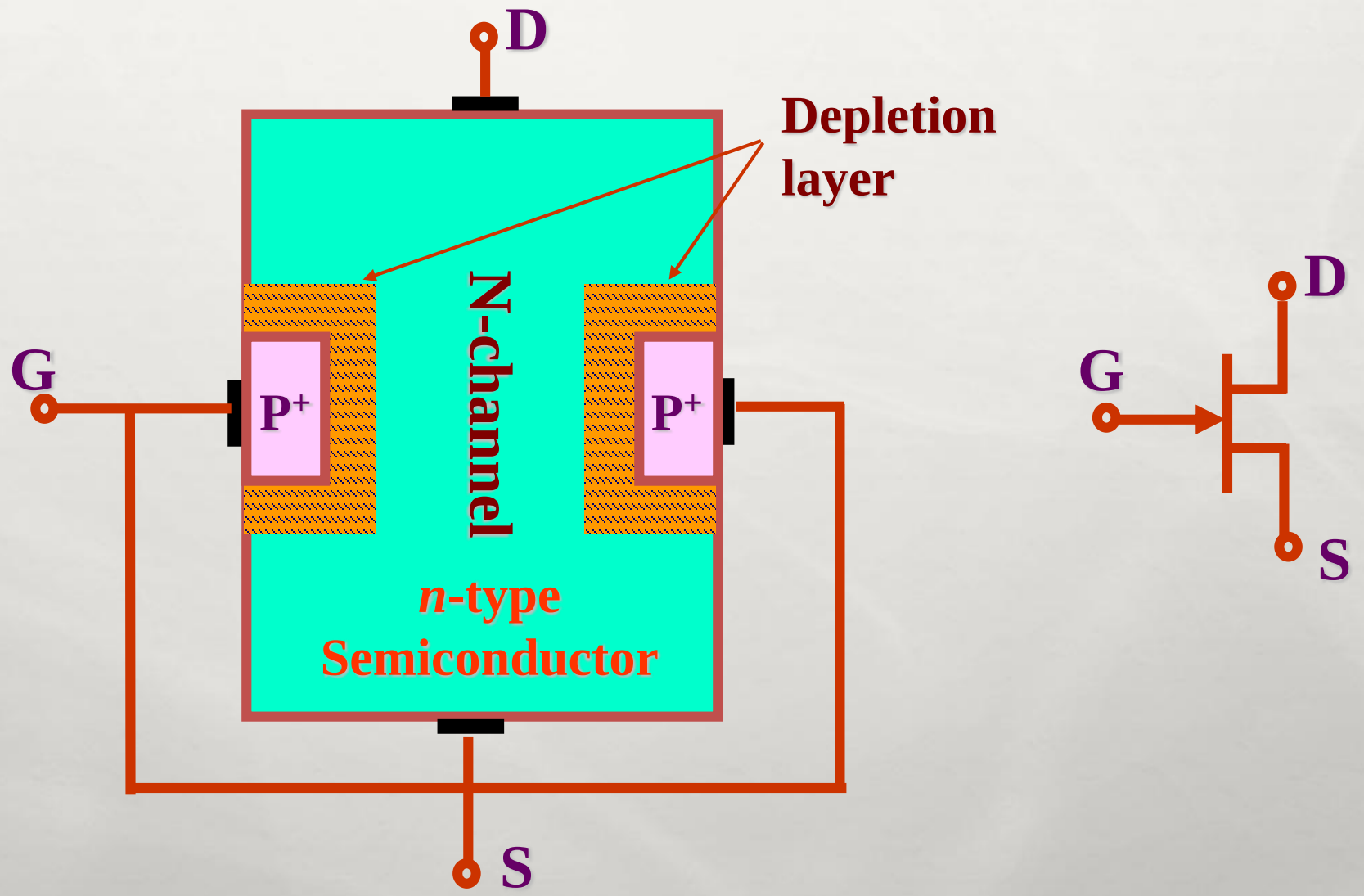
JFET drain curves

OPERASI JFET

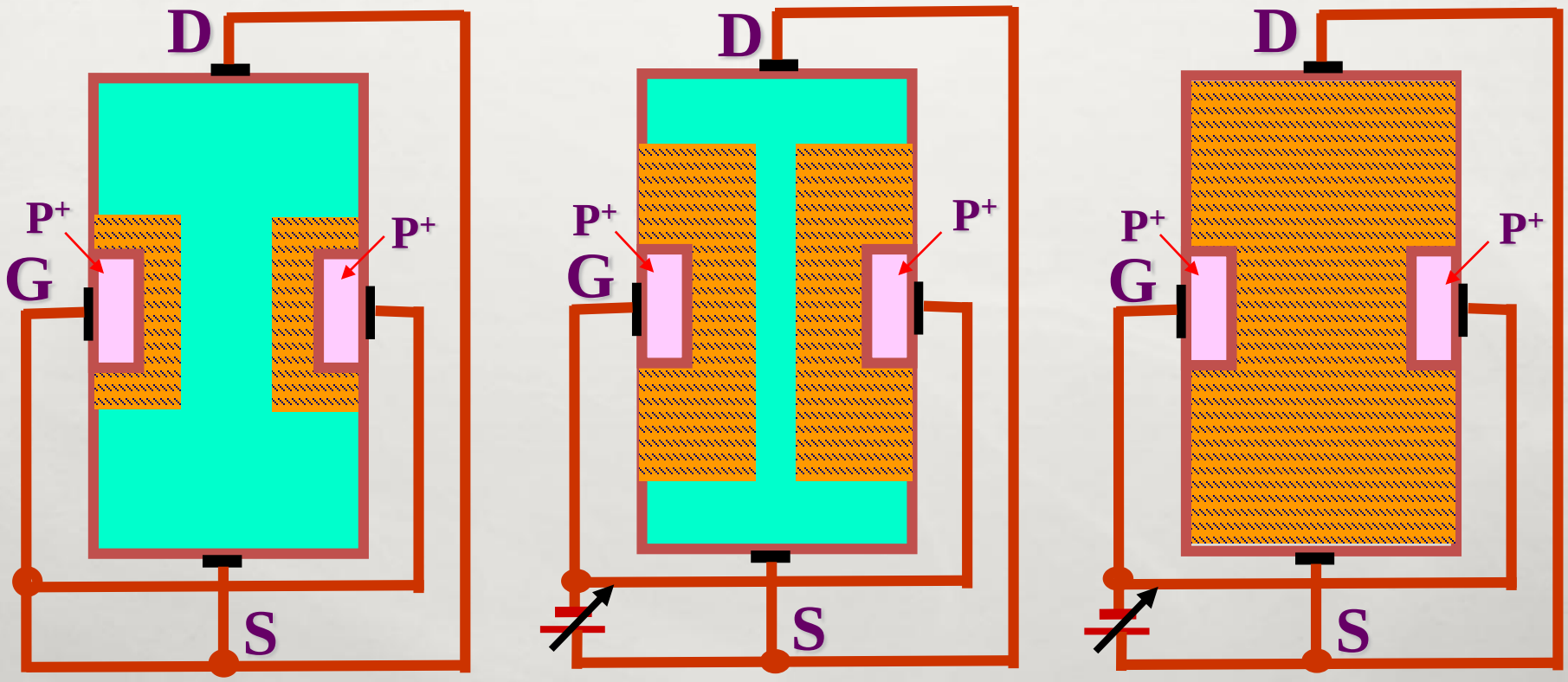




JUNCTION FET

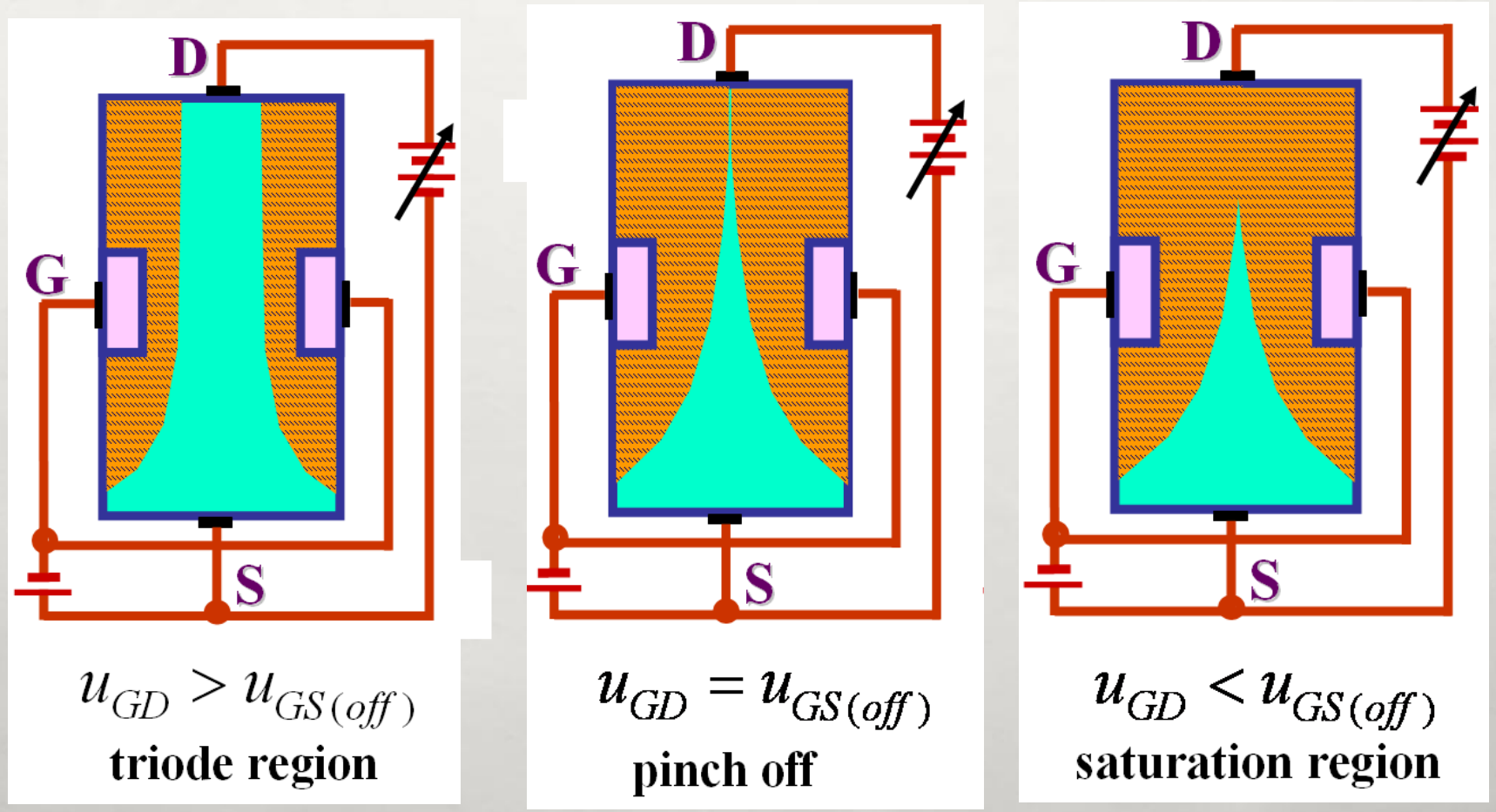


PHYSICAL OPERATION UNDER V_{DS}=0

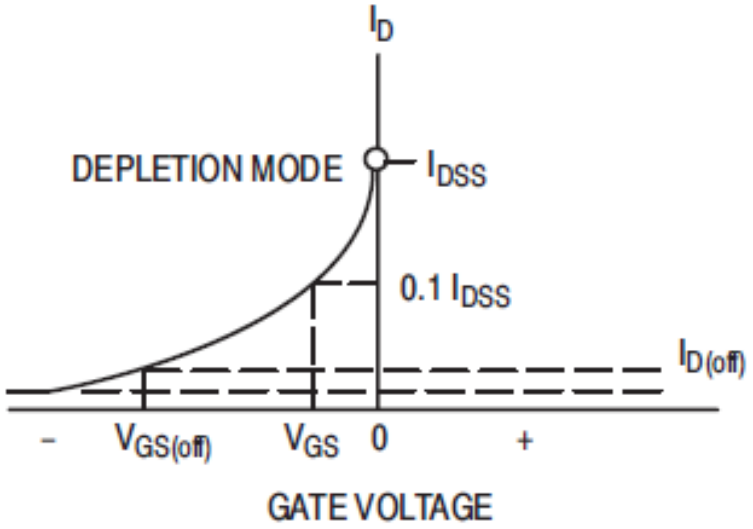


$U_{GS} = 0$ $U_{GS} < 0$ $U_{GS} = U_{GS(off)}$

The effect of U_{DS} on I_D for $U_{GS(off)} < U_{GS} < 0$

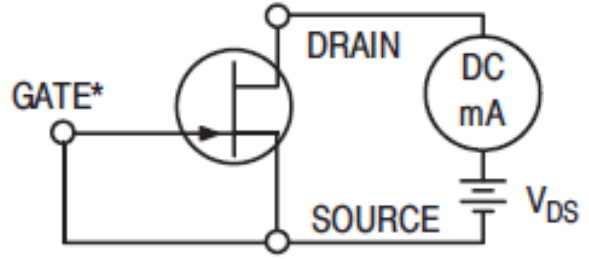


TEST

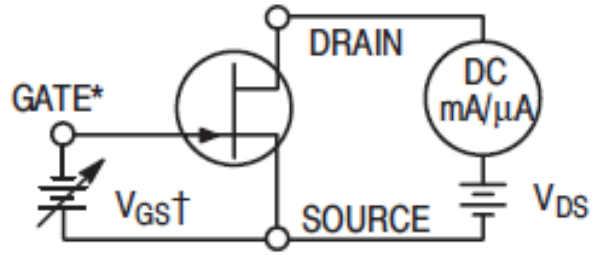


DEPLETION MODE JFETs

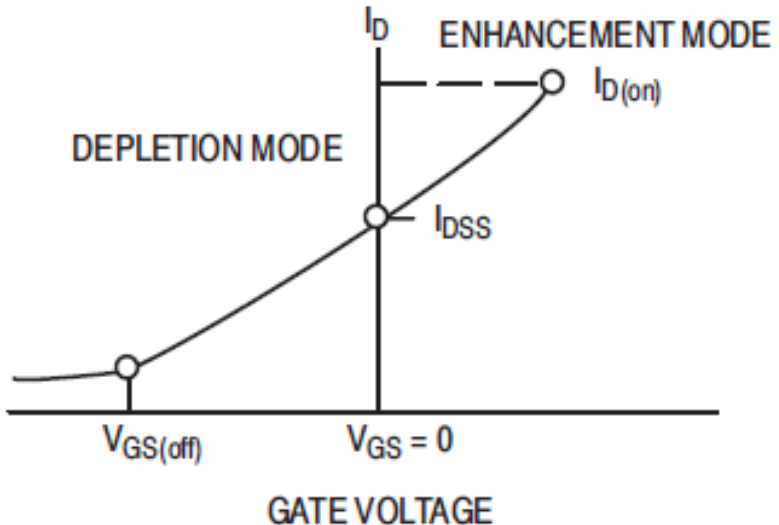
CHARACTERISTIC	DESCRIPTION
I_{DSS} @ V_{GS} = 0, $V_P < V_{DS} < V_{(BR)DSS}$	Zero-gate-voltage drain current. Represents maximum drain current.
$V_{GS(off)}$ @ I_D = 0.001 I_{DSS}, $V_P < V_{DS} < V_{(BR)DSS}$	Gate voltage necessary to reduce I_D to some specified negligible value at the recommended V_{DS} i.e. cutoff.
V_{GS} @ I_D = 0.1 I_{DSS}, $V_P < V_{DS} < V_{(BR)DSS}$	Gate voltage for a specified value of I_D between I_{DSS} and I_{DS} at cutoff – normally 0.1 I_{DSS}.



TEST CIRCUIT FOR I_{DSS}

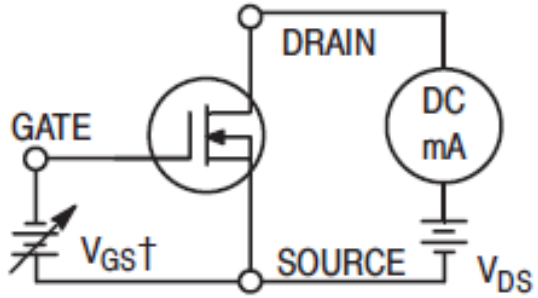


TEST CIRCUIT FOR V_{GS} AND $V_{GS(off)}$
* GATES INTERNALLY CONNECTED
† ADJUST FOR DESIRED I_D



DEPLETION/ENHANCEMENT MODE MOSFETs

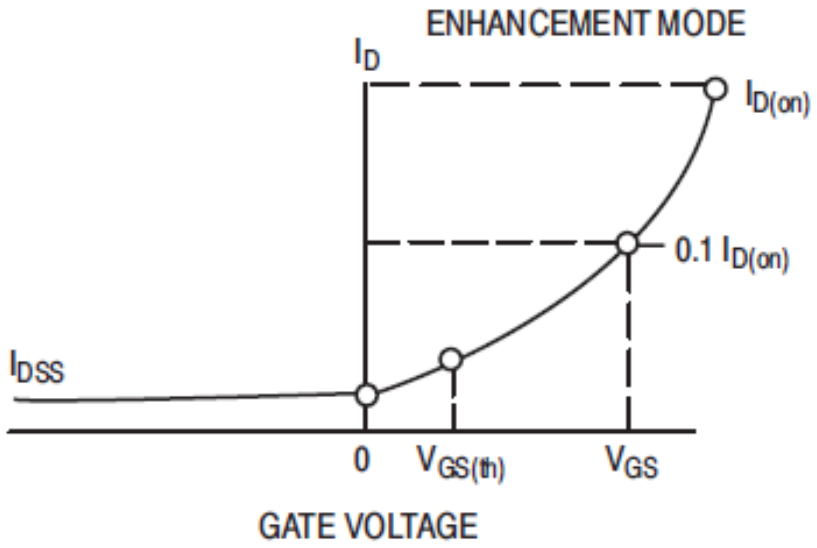
CHARACTERISTIC	DESCRIPTION
$I_{D(on)}$ @ V_{GS} > 0, $V_P < V_{DS} < V_{(BR)DSS}$	An arbitrary current value (usually near max rated current) that locates a point in the enhancement operation mode.
I_{DSS} @ V_{GS} = 0, $V_P < V_{DS} < V_{(BR)DSS}$	Zero-gate-voltage drain current.
$V_{GS(off)}$ @ I_D = 0.001 I_{DSS}	Voltage necessary to reduce I_D to some specified negligible value at the recommended V_{DS}, i.e. cutoff.



TEST CIRCUIT FOR $I_{D(on)}$
† ADJUST FOR DESIRED I_D,
NORMALLY NEAR MAX-RATED I_D

TEST CIRCUIT FOR I_{DSS} AND $V_{GS(off)}$

TEST MODE ENHANCEMENT



ENHANCEMENT MODE MOSFETs

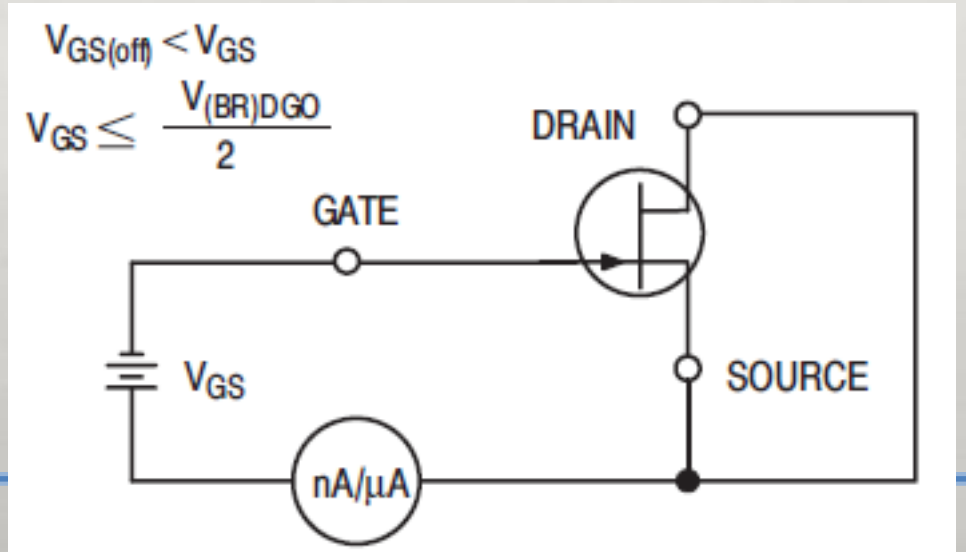
CHARACTERISTIC	DESCRIPTION
$I_{D(on)}$ @ $V_{GS} > 0$, $V_P < V_{DS} < V_{(BR)DSS}$	An arbitrary current value (usually near max rated current) that locates a point in the enhancement operation mode.
V_{GS} @ 0.1 $I_{D(on)}$	Gate-source voltage for a specified drain current of 0.1 $I_{D(on)}$.
$V_{GS(th)}$ @ I_D = 0.001 $I_{D(on)}$ or less	Gate cutoff or turn-on voltage.
I_{DSS} @ V_{GS} = 0, $V_P < V_{DS} < V_{(BR)DSS}$	Leakage drain current.

$I_{D(on)}$ TEST CIRCUIT
SAME AS FOR DEPLETION/ ENHANCEMENT

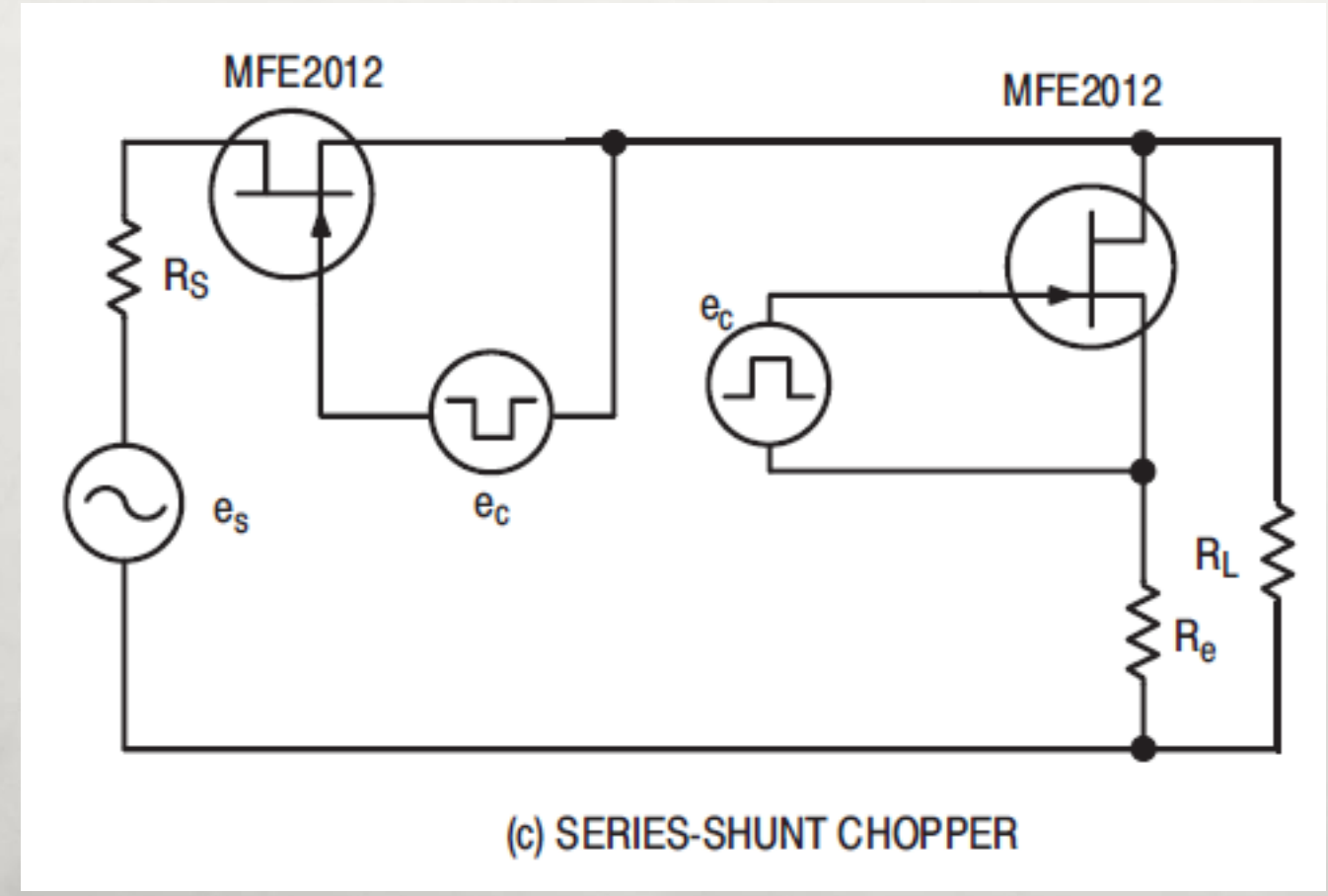
V_{GS} TEST CIRCUIT
SAME AS FOR $I_{D(on)}$

$V_{GS(th)}$ TEST CIRCUIT
SAME AS FOR $V_{GS(off)}$ FOR JFET EXCEPT REVERSE V_{GS} BATTERY POLARITY

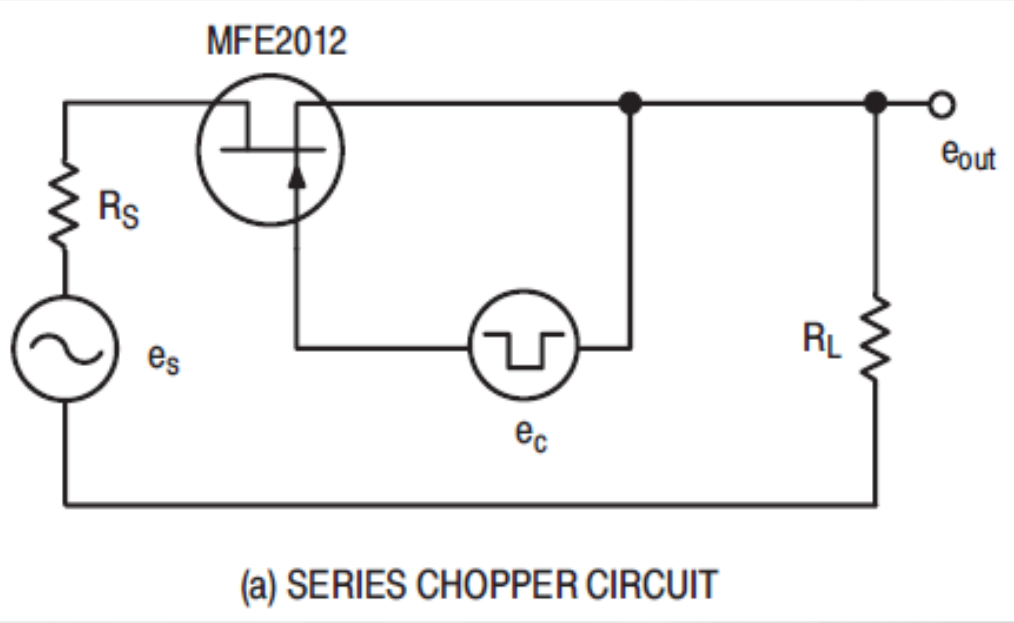
I_{DSS} TEST CIRCUIT
SAME AS FOR JFET



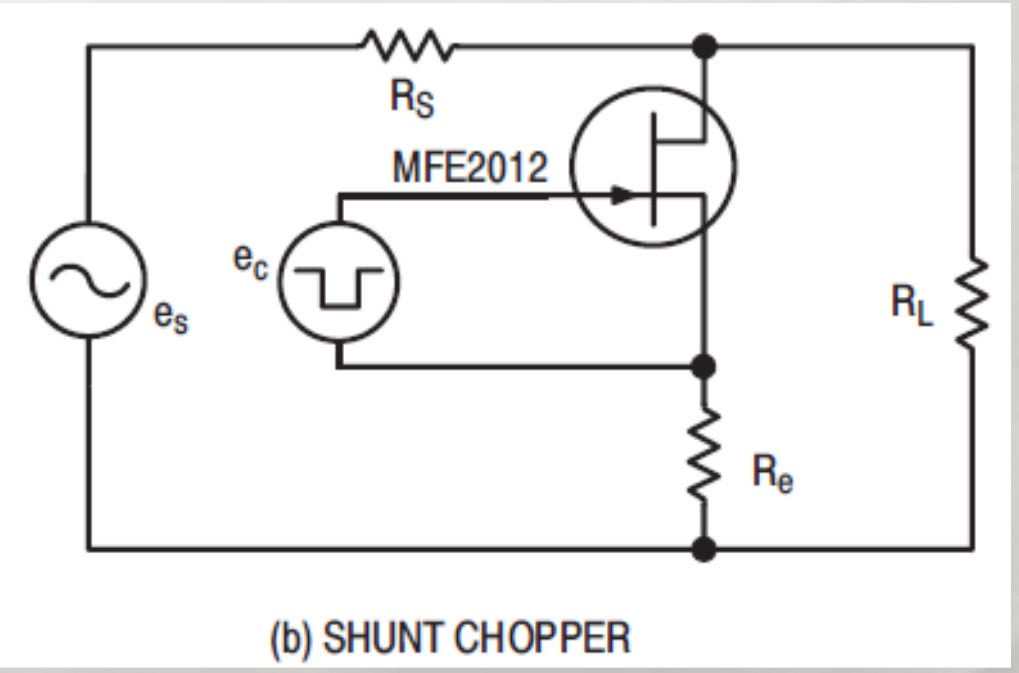
RANGKAIAN COPER FET



(c) SERIES-SHUNT CHOPPER



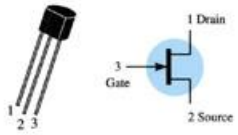
(a) SERIES CHOPPER CIRCUIT



(b) SHUNT CHOPPER

Specification Sheet (JFETs)

2N5457
CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFETs
GENERAL PURPOSE
N-CHANNEL—DEPLETION

Refer to 2N4220 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

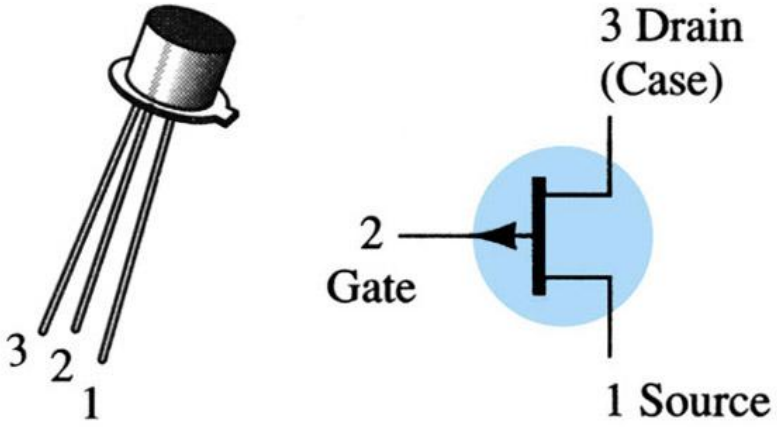
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage (I_G = –10 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	–25	–	–	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc, V_{DS} = 0) (V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 100°C)		I_{GSS}	– –	– –	–1.0 –200	nAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5457	$V_{GS(off)}$	–0.5	–	–6.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 100 μAdc)	2N5457	V_{GS}	–	–2.5	–	Vdc
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current* (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5457	$\|y_{fs}\|$	1000	–	5000	μmhos
Output Admittance Common Source* (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	–	10	50	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	–	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	–	1.5	3.0	pF

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

CASE CONSTRUCTION AND TERMINAL IDENTIFICATION

2N2844

CASE 22-03, STYLE 12
TO-18 (TO-206AA)



JFETs
GENERAL PURPOSE
P-CHANNEL

IRFZ44 DATASHEET

Advanced Power MOSFET

IRFZ44

FEATURES

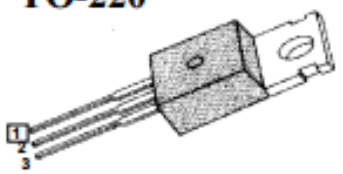
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current: 10μA (Max.) @ V_{DS} = 60V
- Lower $R_{DS(ON)}$: 0.020Ω (Typ.)

BV_{DSS} = 60 V

$R_{DS(on)}$ = 0.024Ω

I_D = 50 A

TO-220

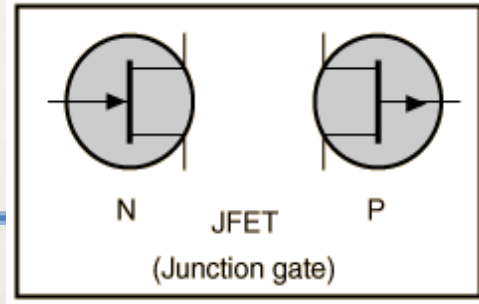


1.Gate 2. Drain 3. Source

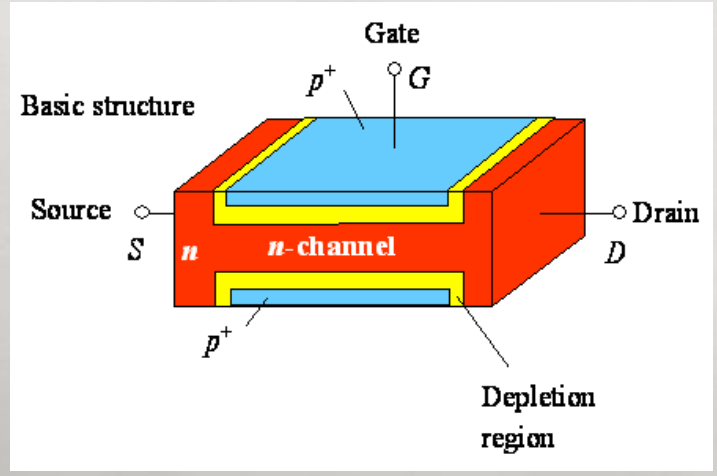
Absolute Maximum Ratings

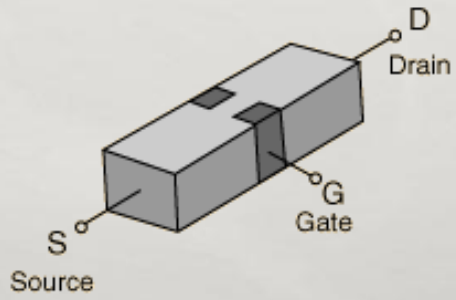
Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current (T_C=25°C)	50	A
	Continuous Drain Current (T_C=100°C)	35.4	
I_{DM}	Drain Current-Pulsed (1)	200	A
V_{GS}	Gate-to-Source Voltage	±20	V

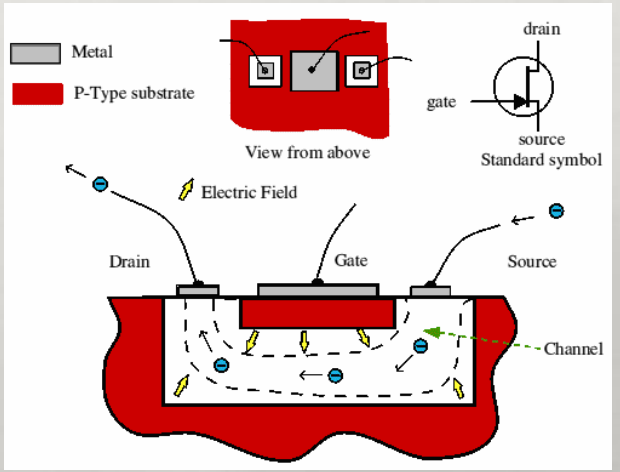
JUNCTION FETS (JFETS)



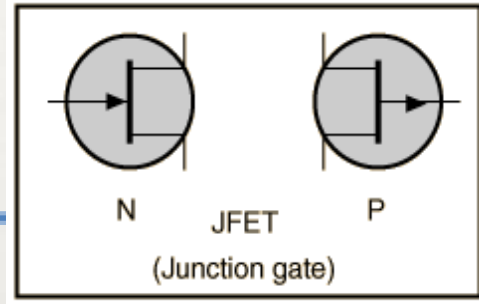
- JFETS CONSISTS OF A PIECE OF HIGH-RESISTIVITY SEMICONDUCTOR MATERIAL (USUALLY SI) WHICH CONSTITUTES A CHANNEL FOR THE MAJORITY CARRIER FLOW.
- CONDUCTING SEMICONDUCTOR CHANNEL BETWEEN TWO OHMIC CONTACTS – SOURCE & DRAIN



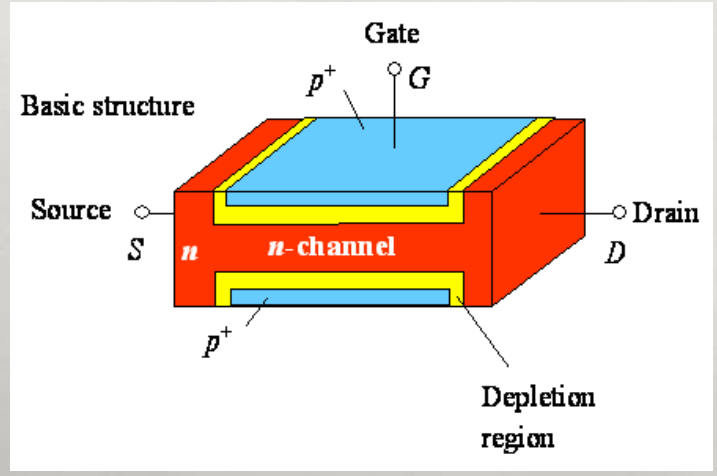


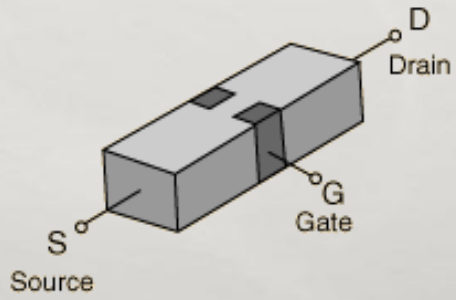


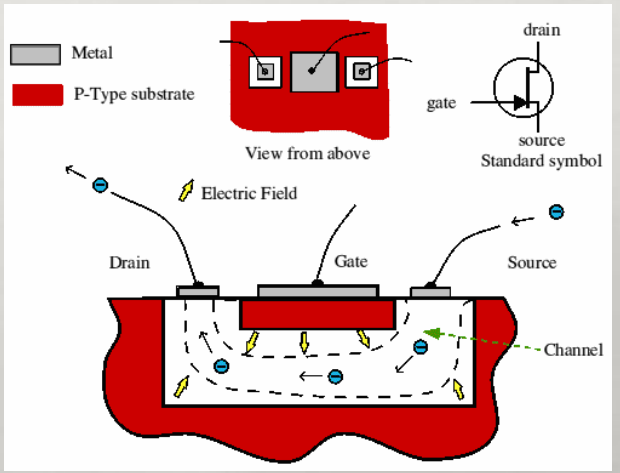
JUNCTION FETS (JFETS)



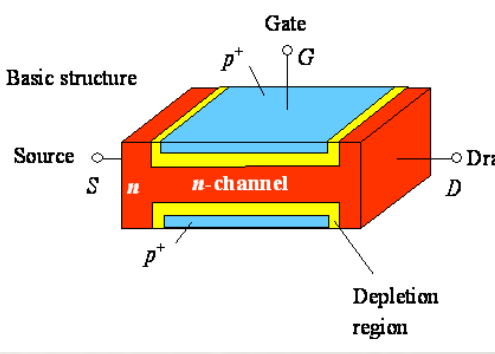
- THE MAGNITUDE OF THIS CURRENT IS CONTROLLED BY A VOLTAGE APPLIED TO A GATE, WHICH IS A REVERSE-BIASED.
- THE FUNDAMENTAL DIFFERENCE BETWEEN JFET AND BJT DEVICES: WHEN THE JFET JUNCTION IS REVERSE-BIASED THE GATE CURRENT IS PRACTICALLY ZERO, WHEREAS THE BASE CURRENT OF THE BJT IS ALWAYS SOME VALUE GREATER THAN ZERO.





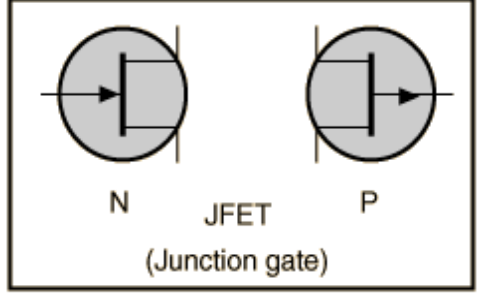


JUNCTION FETS

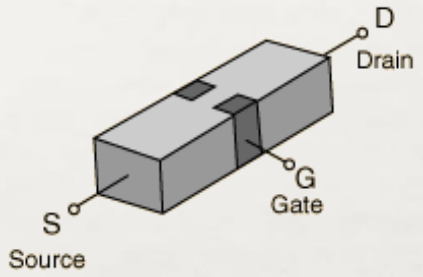


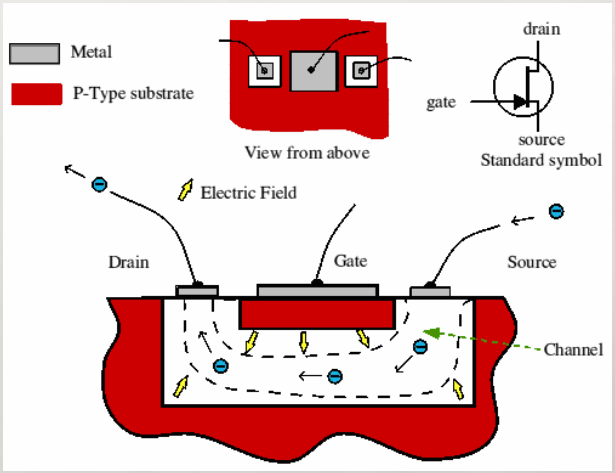
- JFET IS A HIGH-INPUT RESISTANCE DEVICE, WHILE THE BJT IS COMPARATIVELY LOW.
- IF THE CHANNEL IS DOPED WITH A DONOR IMPURITY, N-TYPE MATERIAL IS FORMED AND THE CHANNEL CURRENT WILL CONSIST OF ELECTRONS.
- IF THE CHANNEL IS DOPED WITH AN ACCEPTOR IMPURITY, P-TYPE MATERIAL WILL BE FORMED AND THE CHANNEL CURRENT WILL CONSIST OF HOLES.
- N-CHANNEL DEVICES HAVE GREATER CONDUCTIVITY THAN P-CHANNEL TYPES, SINCE ELECTRONS HAVE HIGHER MOBILITY THAN DO HOLES; THUS N-CHANNEL JFETS ARE APPROXIMATELY TWICE AS EFFICIENT CONDUCTORS COMPARED TO THEIR P-CHANNEL COUNTERPARTS.

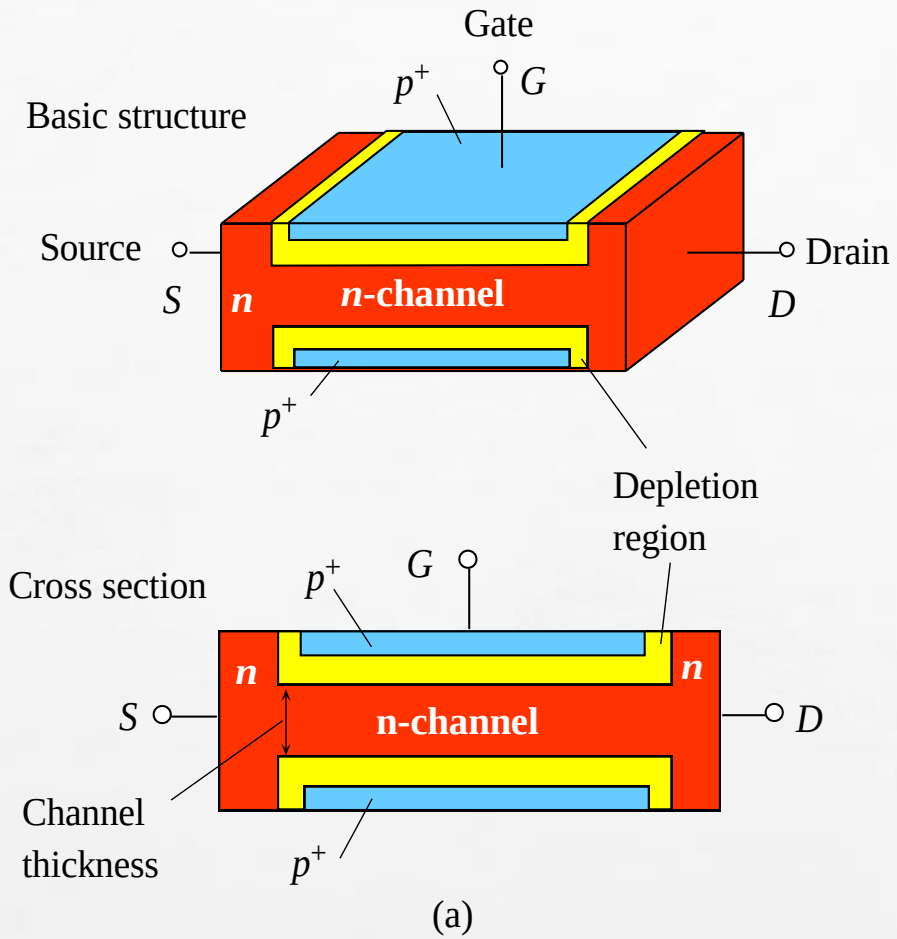
BASIC STRUCTURE OF JFETS

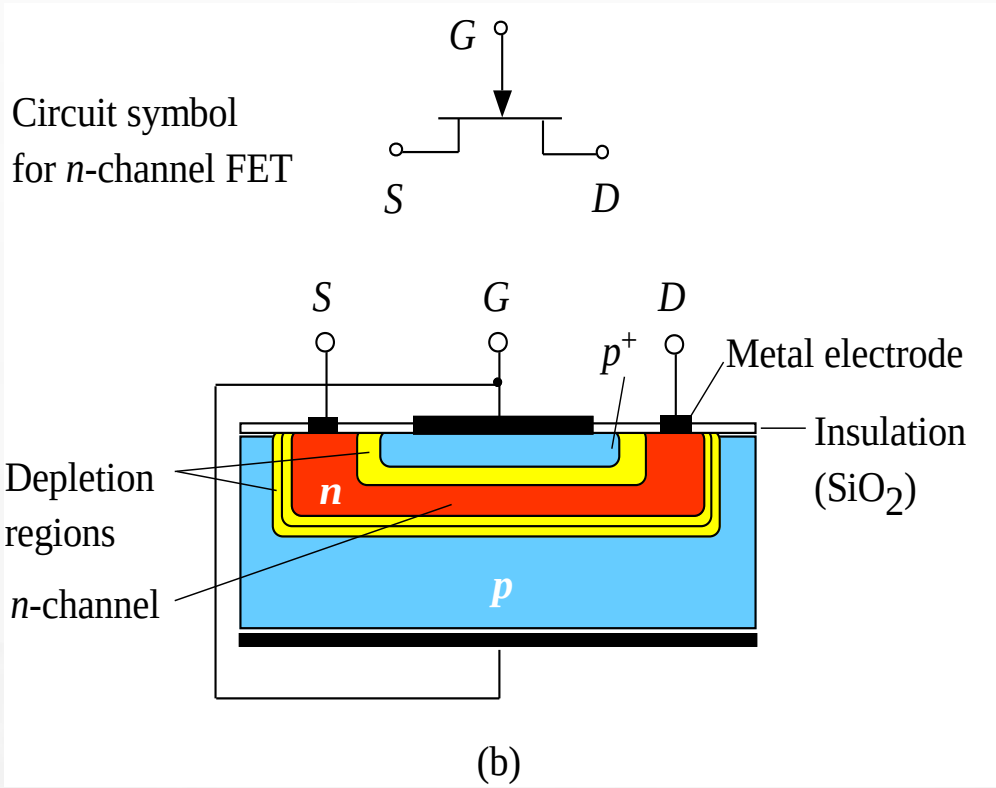


- IN ADDITION TO THE CHANNEL, A JFET CONTAINS TWO OHMIC CONTACTS: THE SOURCE AND THE DRAIN.
- THE JFET WILL CONDUCT CURRENT EQUALLY WELL IN EITHER DIRECTION AND THE SOURCE AND DRAIN LEADS ARE USUALLY INTERCHANGEABLE.





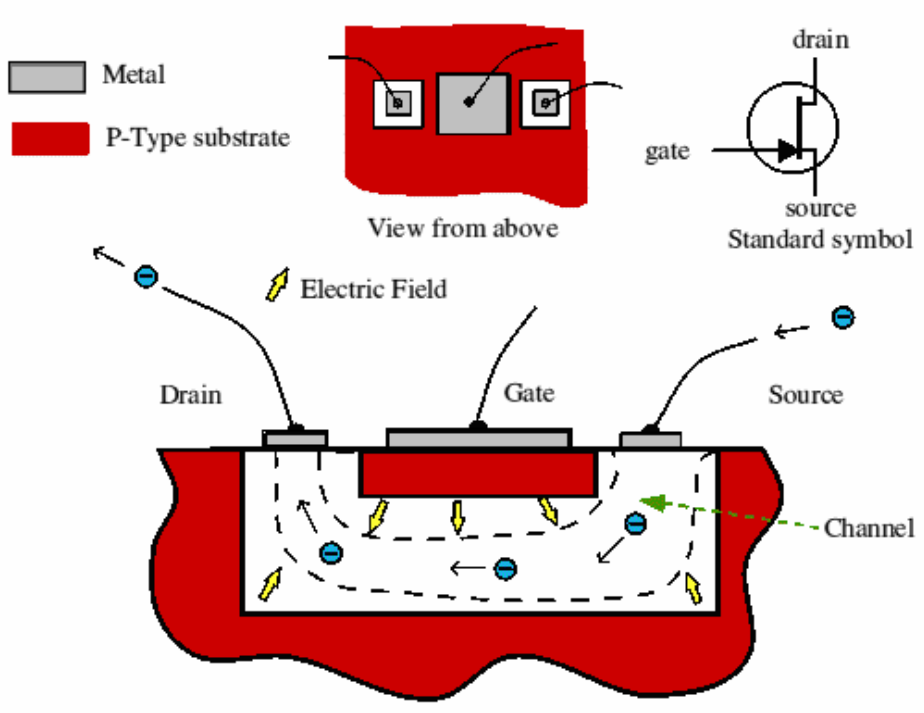




(a)The basic structure of the junction field effect transistor (JFET) with an *n*-channel. The two p^+ regions are electrically connected and form the gate. (b) A simplified sketch of the cross section of a more practical *n*-channel JFET.

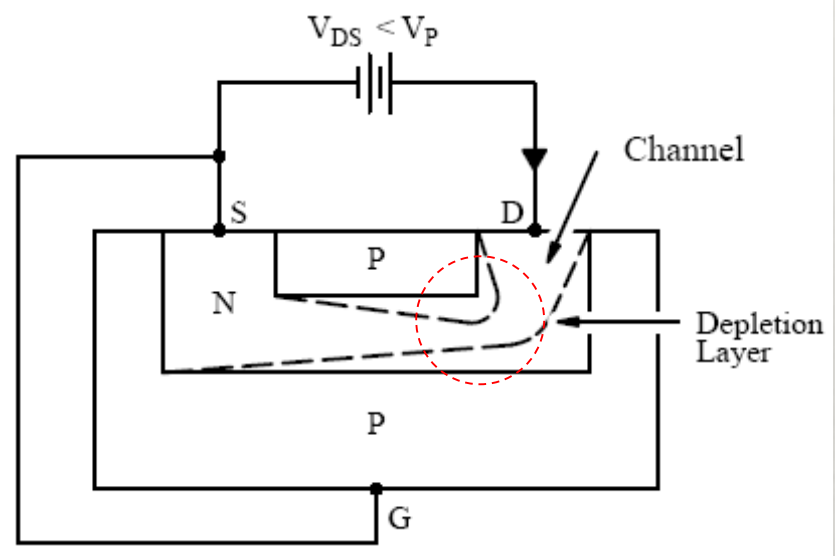
N-CHANNEL JFET

- THIS TRANSISTOR IS MADE BY FORMING A CHANNEL OF N-TYPE MATERIAL IN A *P-TYPE SUBSTRATE.*
- THREE WIRES ARE THEN CONNECTED TO THE DEVICE.
- ONE AT EACH END OF THE CHANNEL.
- ONE CONNECTED TO THE SUBSTRATE.
- IN A SENSE, THE DEVICE IS A BIT LIKE A PN-JUNCTION DIODE, EXCEPT THAT THERE ARE TWO WIRES CONNECTED TO THE N-TYPE SIDE.



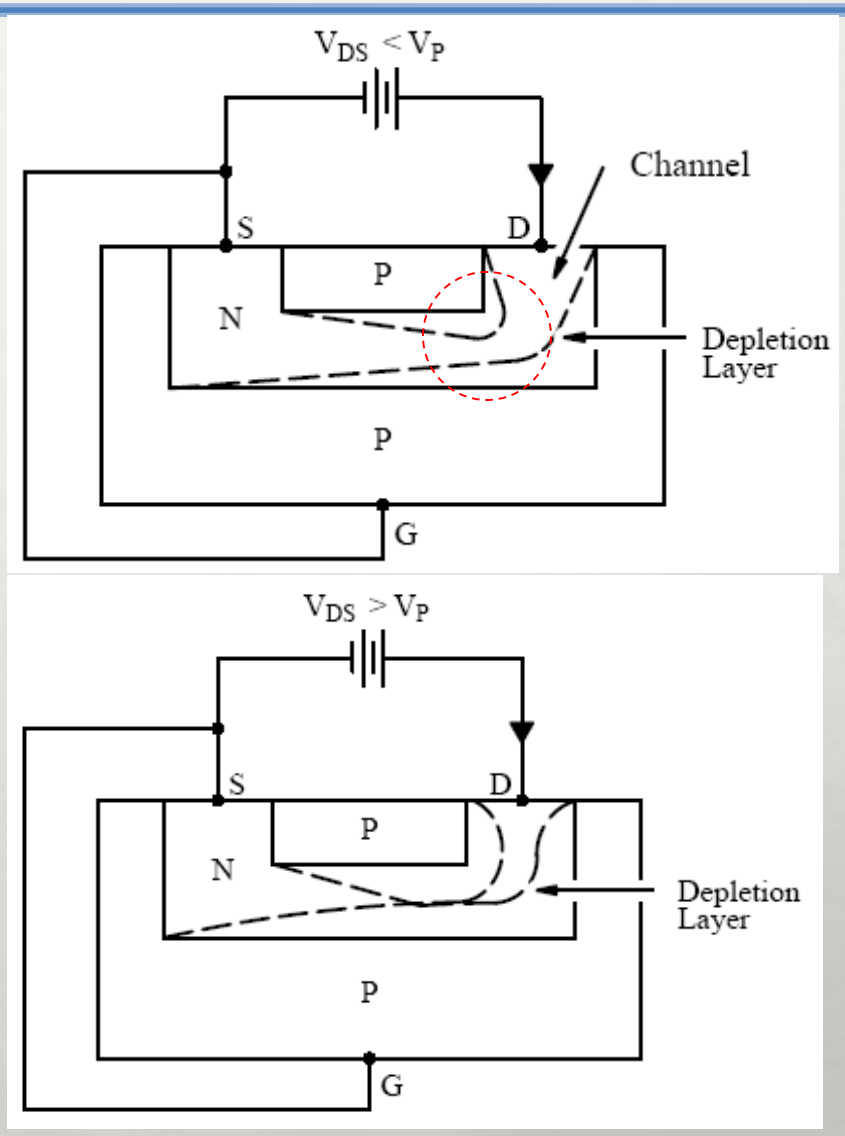
HOW JFET FUNCTION

- THE GATE IS CONNECTED TO THE SOURCE.
- SINCE THE PN JUNCTION IS REVERSE-BIASED, LITTLE CURRENT WILL FLOW IN THE GATE CONNECTION.
- THE POTENTIAL GRADIENT ESTABLISHED WILL FORM A DEPLETION LAYER, WHERE ALMOST ALL THE ELECTRONS PRESENT IN THE N-TYPE CHANNEL WILL BE SWEPT AWAY.
- THE MOST DEPLETED PORTION IS IN THE HIGH FIELD BETWEEN THE G AND THE D, AND THE LEAST-DEPLETED AREA IS BETWEEN THE G AND THE S.

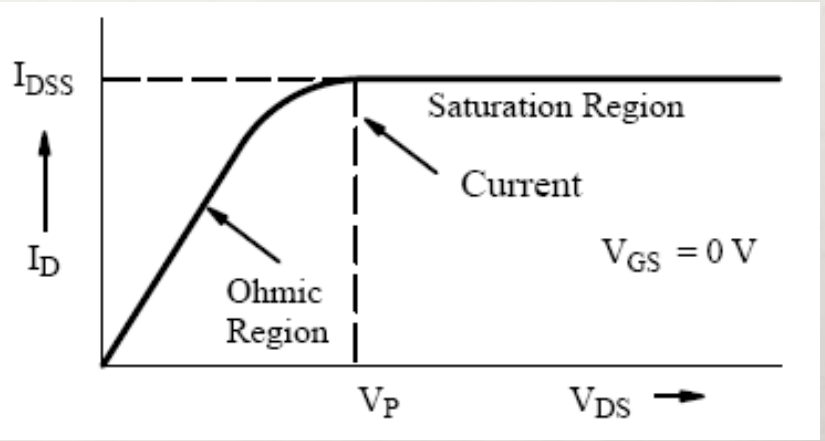


HOW JFET FUNCTION

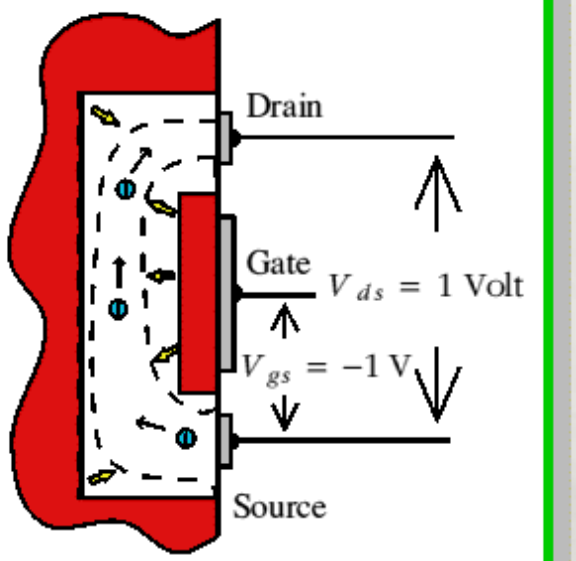
- BECAUSE THE FLOW OF CURRENT ALONG THE CHANNEL FROM THE (+VE) DRAIN TO THE (-VE) SOURCE IS REALLY A FLOW OF FREE ELECTRONS FROM S TO D IN THE N-TYPE SI, THE MAGNITUDE OF THIS CURRENT WILL FALL AS MORE SI BECOMES DEPLETED OF FREE ELECTRONS.
- THERE IS A LIMIT TO THE DRAIN CURRENT (I_D) WHICH INCREASED V_{DS} CAN DRIVE THROUGH THE CHANNEL.
- THIS LIMITING CURRENT IS KNOWN AS I_{DSS} (*DRAIN-TO-SOURCE CURRENT WITH THE GATE SHORTED TO THE SOURCE*).



- THE OUTPUT CHARACTERISTICS OF AN N-CHANNEL JFET WITH THE GATE SHORT-CIRCUITED TO THE SOURCE.
- THE INITIAL RISE IN I_D IS RELATED TO THE BUILDUP OF THE DEPLETION LAYER AS V_{DS} INCREASES.
- THE CURVE APPROACHES THE LEVEL OF THE LIMITING CURRENT I_{DSS} WHEN I_D BEGINS TO BE PINCHED OFF.
- THE PHYSICAL MEANING OF THIS TERM LEADS TO ONE DEFINITION OF PINCH-OFF VOLTAGE, V_P , WHICH IS THE VALUE OF V_{DS} AT WHICH THE MAXIMUM I_{DSS} FLOWS.

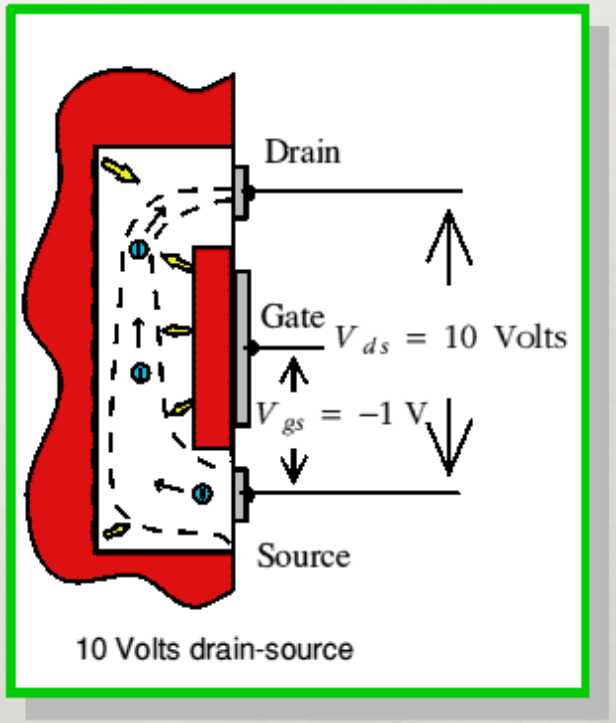


- WITH A STEADY GATE-SOURCE VOLTAGE OF 1 V THERE IS ALWAYS 1 V ACROSS THE WALL OF THE CHANNEL AT THE SOURCE END.
- A DRAIN-SOURCE VOLTAGE OF 1 V MEANS THAT THERE WILL BE 2 V ACROSS THE WALL AT THE DRAIN END. (*THE DRAIN IS 'UP' 1V FROM THE SOURCE POTENTIAL AND THE GATE IS 1V 'DOWN', HENCE THE TOTAL DIFFERENCE IS 2V.)*
- THE HIGHER VOLTAGE DIFFERENCE AT THE DRAIN END MEANS THAT THE ELECTRON CHANNEL IS SQUEEZED DOWN A BIT MORE AT THIS END.

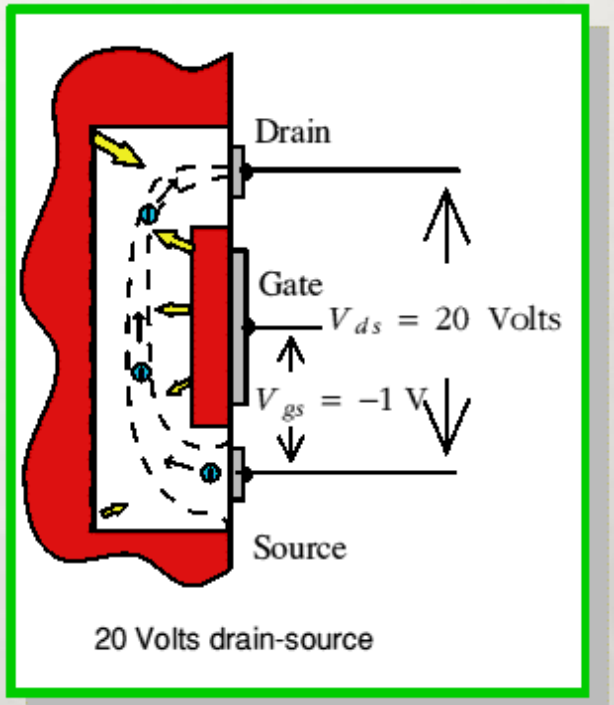


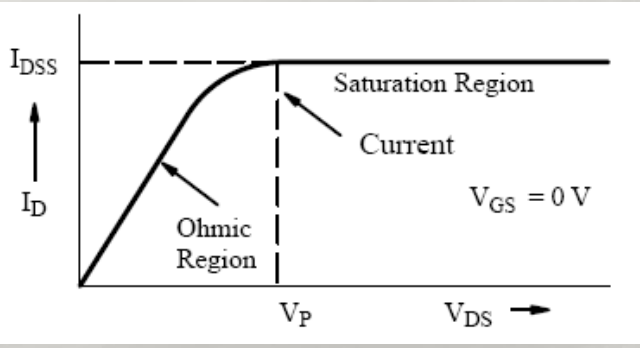
1 Volt drain-source

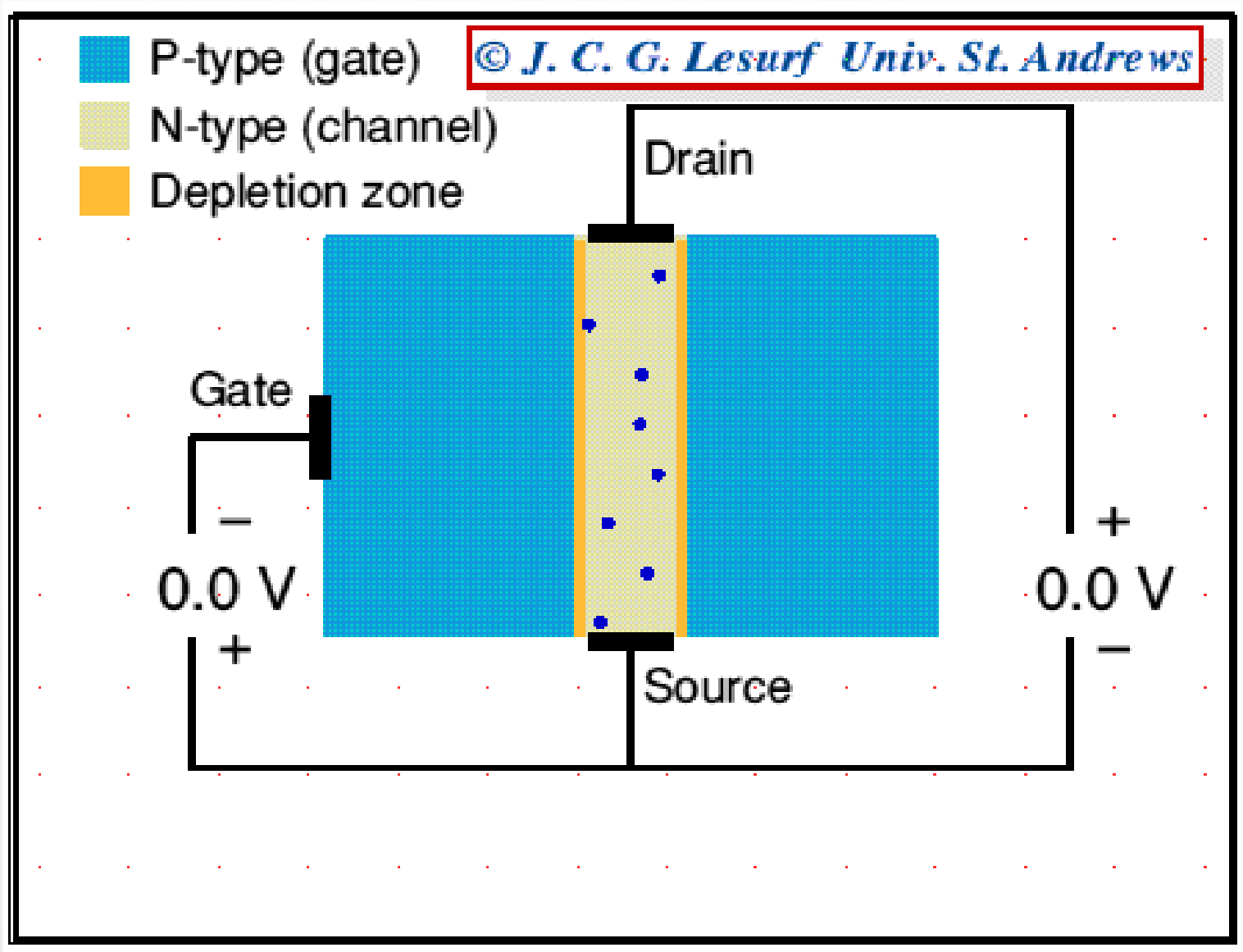
- WHEN THE DRAIN-SOURCE VOLTAGE IS INCREASED TO 10V THE VOLTAGE ACROSS THE CHANNEL WALLS AT THE DRAIN END INCREASES TO 11V, BUT REMAINS JUST 1V AT THE SOURCE END.
- THE FIELD ACROSS THE WALLS NEAR THE DRAIN END IS NOW A LOT LARGER THAN AT THE SOURCE END.
- AS A RESULT THE CHANNEL NEAR THE DRAIN IS SQUEEZED DOWN QUITE A LOT.



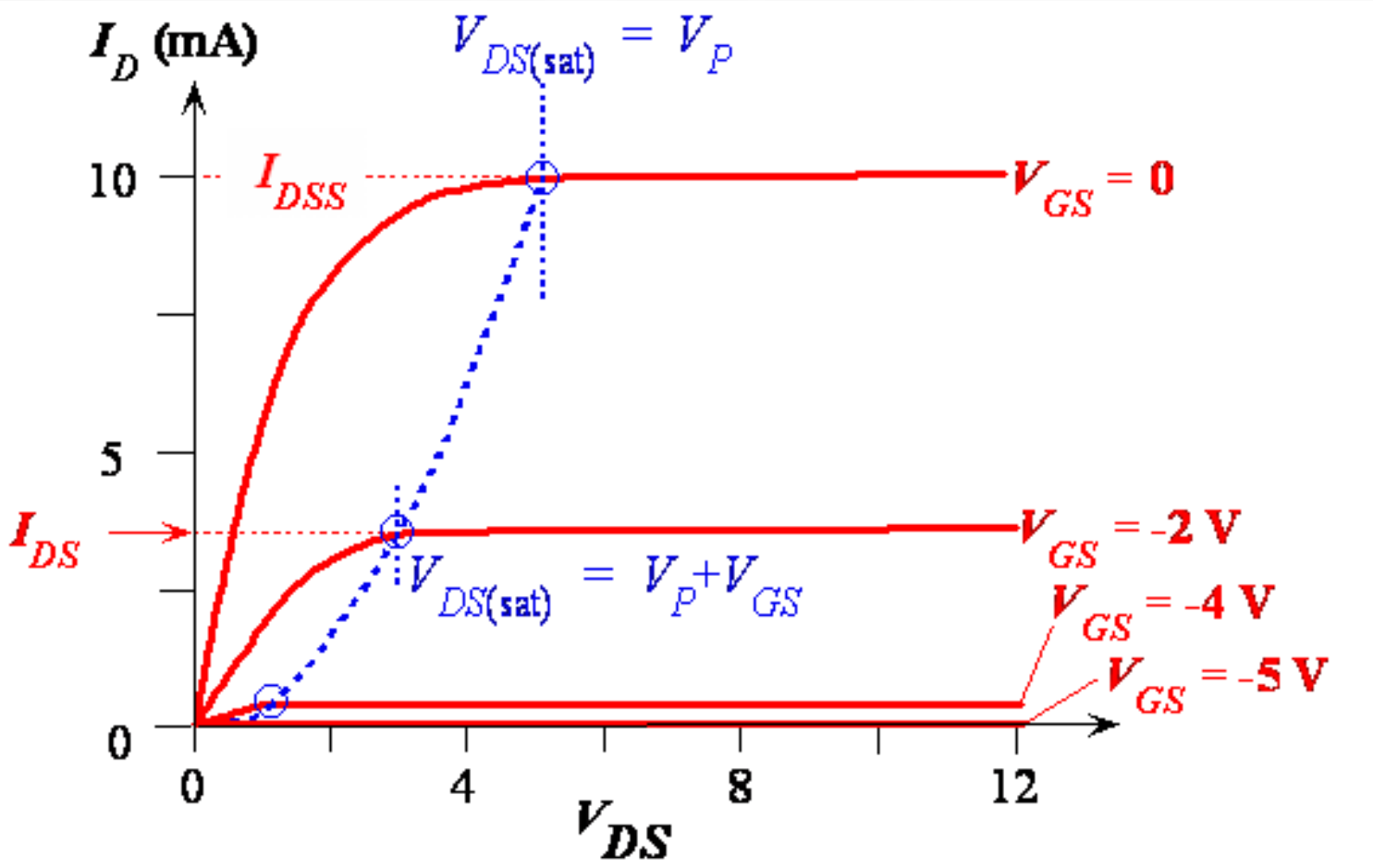
- INCREASING THE SOURCE-DRAIN VOLTAGE TO 20V SQUEEZES DOWN THIS END OF THE CHANNEL STILL MORE.
- AS WE INCREASE THIS VOLTAGE WE INCREASE THE ELECTRIC FIELD WHICH DRIVES ELECTRONS ALONG THE OPEN PART OF THE CHANNEL.
- HOWEVER, ALSO SQUEEZES DOWN THE CHANNEL NEAR THE DRAIN END.
- THIS REDUCTION IN THE OPEN CHANNEL WIDTH MAKES IT HARDER FOR ELECTRONS TO PASS.
- AS A RESULT THE DRAIN-SOURCE CURRENT TENDS TO REMAIN CONSTANT WHEN WE INCREASE THE DRAIN-SOURCE VOLTAGE.





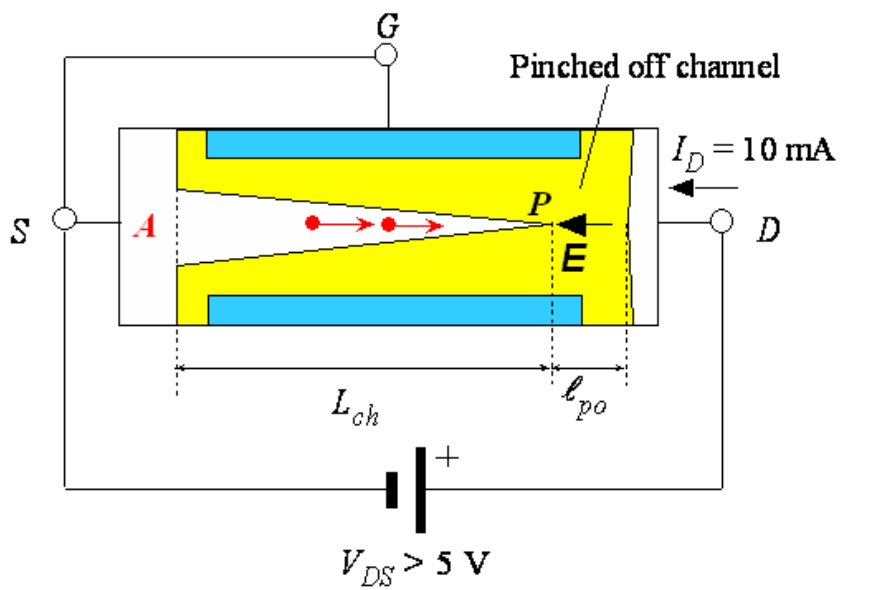

P-type (gate)
N-type (channel)
Depletion zone
© J. C. G. Lesurf Univ. St. Andrews
Drain
Gate
–
0.0 V
+
+
0.0 V
–
Source

- INCREASING V_{DS} INCREASES THE WIDTHS OF DEPLETION LAYERS, WHICH PENETRATE MORE INTO CHANNEL AND HENCE RESULT IN MORE CHANNEL NARROWING TOWARD THE DRAIN.
- THE RESISTANCE OF THE N-CHANNEL, R_{AB} THEREFORE INCREASES WITH V_{DS}.
- THE DRAIN CURRENT: $I_{DS} = V_{DS}/R_{AB}$
- I_D VERSUS V_{DS} EXHIBITS A SUBLINEAR BEHAVIOR, SEE FIGURE FOR $V_{DS} < 5V$.
- THE PINCH-OFF VOLTAGE, V_P IS THE MAGNITUDE OF REVERSE BIAS NEEDED ACROSS THE P^+N JUNCTION TO MAKE THEM JUST TOUCH AT THE DRAIN END.
- SINCE ACTUAL BIAS VOLTAGE ACROSS P^+N JUNCTION AT DRAIN END IS V_{GD}, THE PINCH-OFF OCCUR WHENEVER: $V_{GD} = -V_P$.



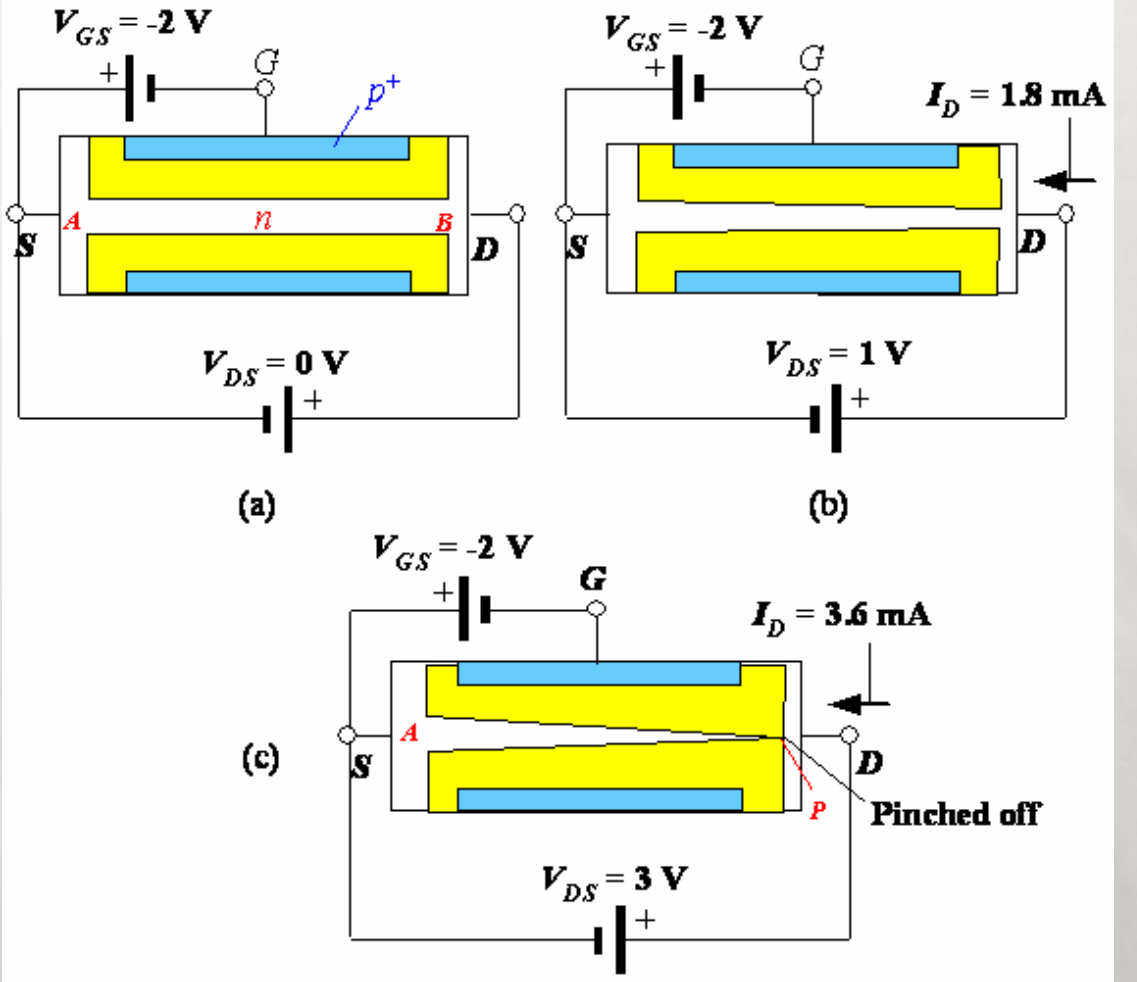
Typical I_D vs V_{DS} characteristics of a JFET for various fixed gate voltages V_{GS}.

- BEYOND $V_{DS} = V_P$, THERE IS A SHORT PINCH-OFF CHANNEL OF LENGTH, ℓ_{PO}.
- AS V_{DS} INCREASES, MOST OF ADDITIONAL VOLTAGE SIMPLY DROPS ACROSS ℓ_{PO} AS THIS REGION IS DEPLETED OF CARRIERS AND HENCE HIGHLY RESISTIVE.
- VOLTAGE DROP ACROSS CHANNEL LENGTH, L_{CH} REMAIN AS V_P.
- BEYOND PINCH-OFF THEN $I_D = V_P/R_{AP}$ ($V_{DS}>V_P$).



The pinched-off channel and conduction for $V_{DS} > V_P$ (=5 V).

- WHAT HAPPEN WHEN NEGATIVE VOLTAGE, SAYS V_{GS} = -2V, IS APPLIED TO GATE WITH RESPECT TO SOURCE (WITH V_{DS}=0).
- THE P^+N JUNCTION ARE NOW REVERSE BIASED FROM THE START, THE CHANNEL IS NARROWER, AND CHANNEL RESISTANCE IS NOW LARGER THAN IN THE V_{GS} = 0 CASE.

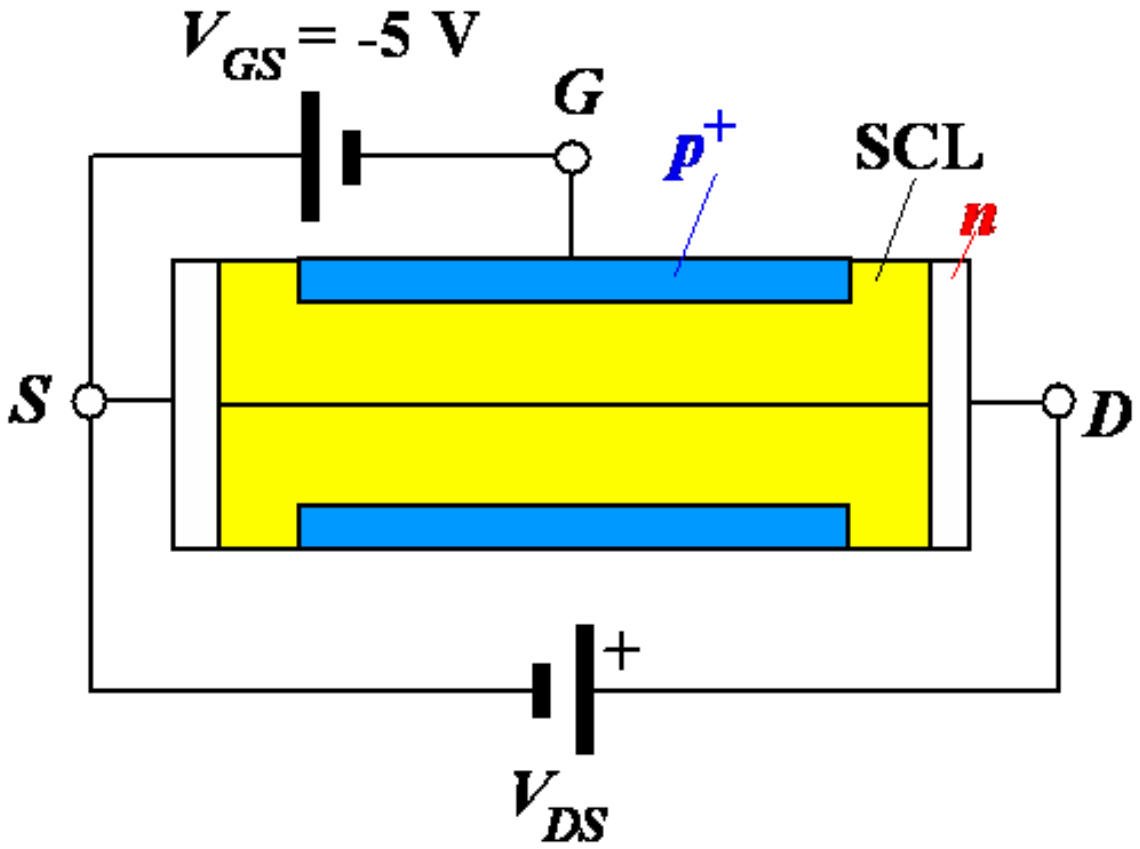


- THE DRAIN CURRENT THAT FLOWS WHEN A SMALL V_{DS} APPLIED (FIG B) IS NOW SMALLER THAN IN V_{GS}= 0 CASE.
- APPLIED V_{DS}= 3 V TO PINCH-OFF THE CHANNEL (FIG C).
- WHEN V_{DS}= 3V, V_{GD} ACROSS $P^{+}N$ JUNCTION AT DRAIN END IS -5V, WHICH IS – V_P, SO CHANNEL BECOMES PINCH-OFF.
- BEYOND PINCH-OFF, I_D IS NEARLY SATURATED JUST AS IN THE V_{GS}=0 CASE.
- PINCH-OFF OCCURS AT V_{DS}= $V_{DS(SAT)}$, $V_{DS(SAT)}$= V_P+V_{GS}, WHERE V_{GS} IS –VE VOLTAGE (REDUCING V_P).
- FOR V_{DS}>$V_{DS(SAT)}$, I_D BECOMES NEARLY SATURATED AT VALUE AS I_{DS}.

- BEYOND PINCH-OF, WITH –VE V_{GS}, I_{DS} IS

$$I_D \approx I_{DS} \approx \frac{V_{DS(sat)}}{R_{AP}(V_{GS})} = \frac{V_P + V_{GS}}{R_{AP}(V_{GS})}, \quad V_{DS} > V_{DS(sat)}$$

- WHERE $R_{AP}(V_{GS})$ IS THE EFFECTIVE RESISTANCE OF THE CONDUCTING N-CHANNEL FROM A TO P, WHICH DEPENDS ON CHANNEL THICKNESS AND HENCE V_{GS}.
- WHEN V_{GS}= -V_P= -5V WITH V_{DS}= 0, THE TWO DEPLETION LAYERS TOUCH OVER THE ENTIRE CHANNEL LENGTH AND THE WHOLE CHANNEL IS CLOSED.
- THE CHANNEL SAID TO BE OFF.



When V_{GS} = -5 V the depletion layers close the whole channel from the start, at V_{DS} = 0. As V_{DS} is increased there is a very small drain current which is the small reverse leakage current due to thermal generation of carriers in the depletion layers.

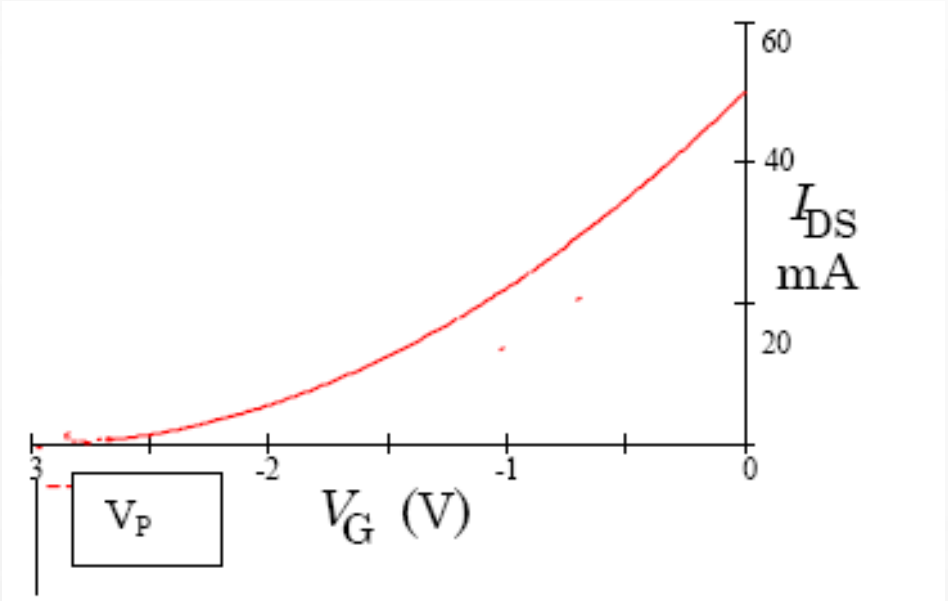
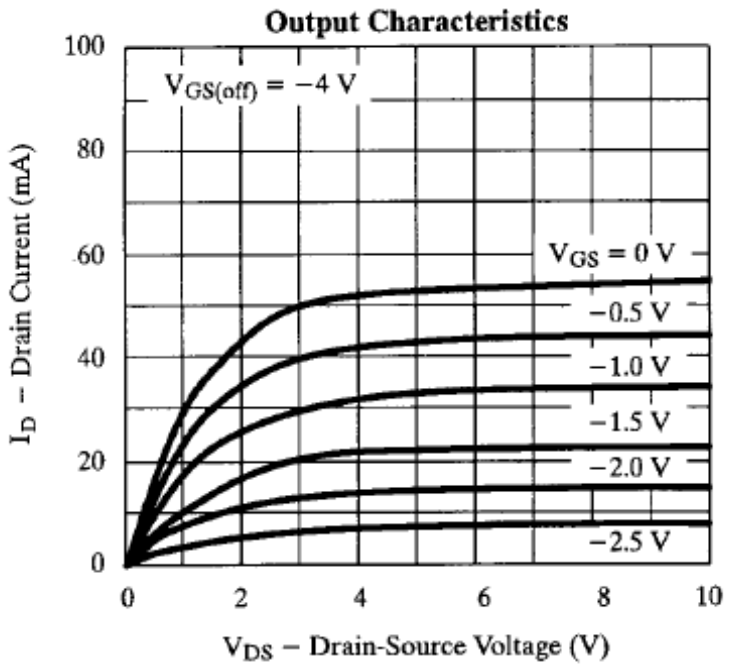
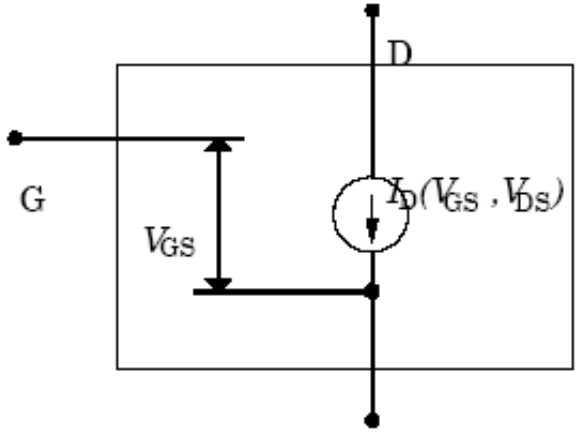


Figure 1: JFET Transfer Characteristic



The source current also depends on the drain source voltage.

A more useful JFET model replaces the variable resistor with a variable current source whose current depends on the gate voltage V_{GS} and the drain-source voltage, V_{DS}.

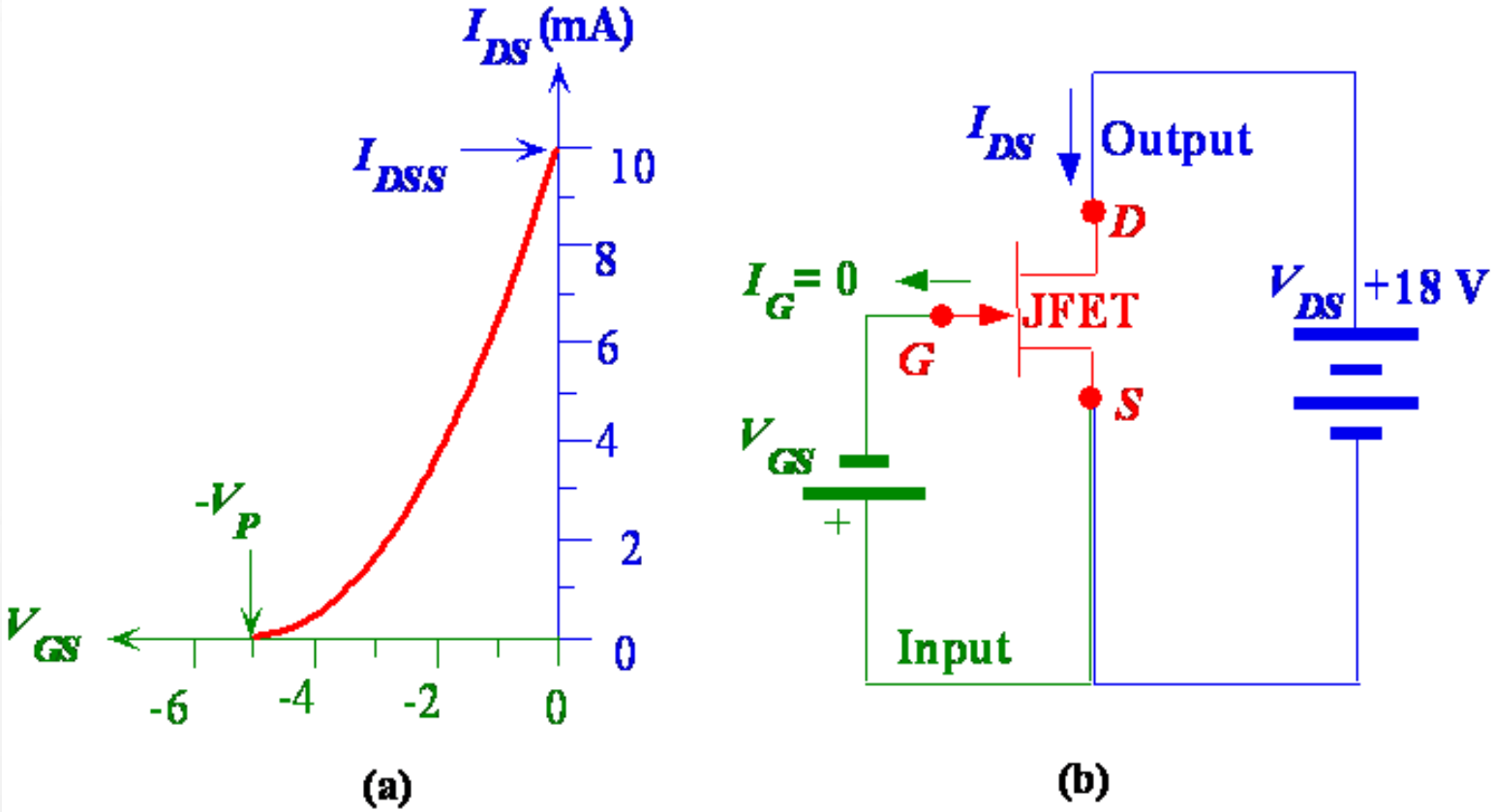


The drain-source current is largest when the gate-source voltage V_{GS} is zero, typically about 50mA. As V_{GS} is made negative, the current decreases. When the gate-source voltage V_{GS} reaches a critical value called the gate-source pinch off voltage V_S, the drain current I_D is cutoff entirely; no current flows. The value of V_S depends on the particular type of JFET (and even varies substantially between JFETs of the same type), but is typically around −4V. As V_{GS} is raised towards 0V, current I_D starts to flow. A typical plot of the current vs. gate voltage is shown in Fig. 1 below. Simple models of JFET performance predict that the curve will be parabolic, but actual devices may differ substantially from this prediction.

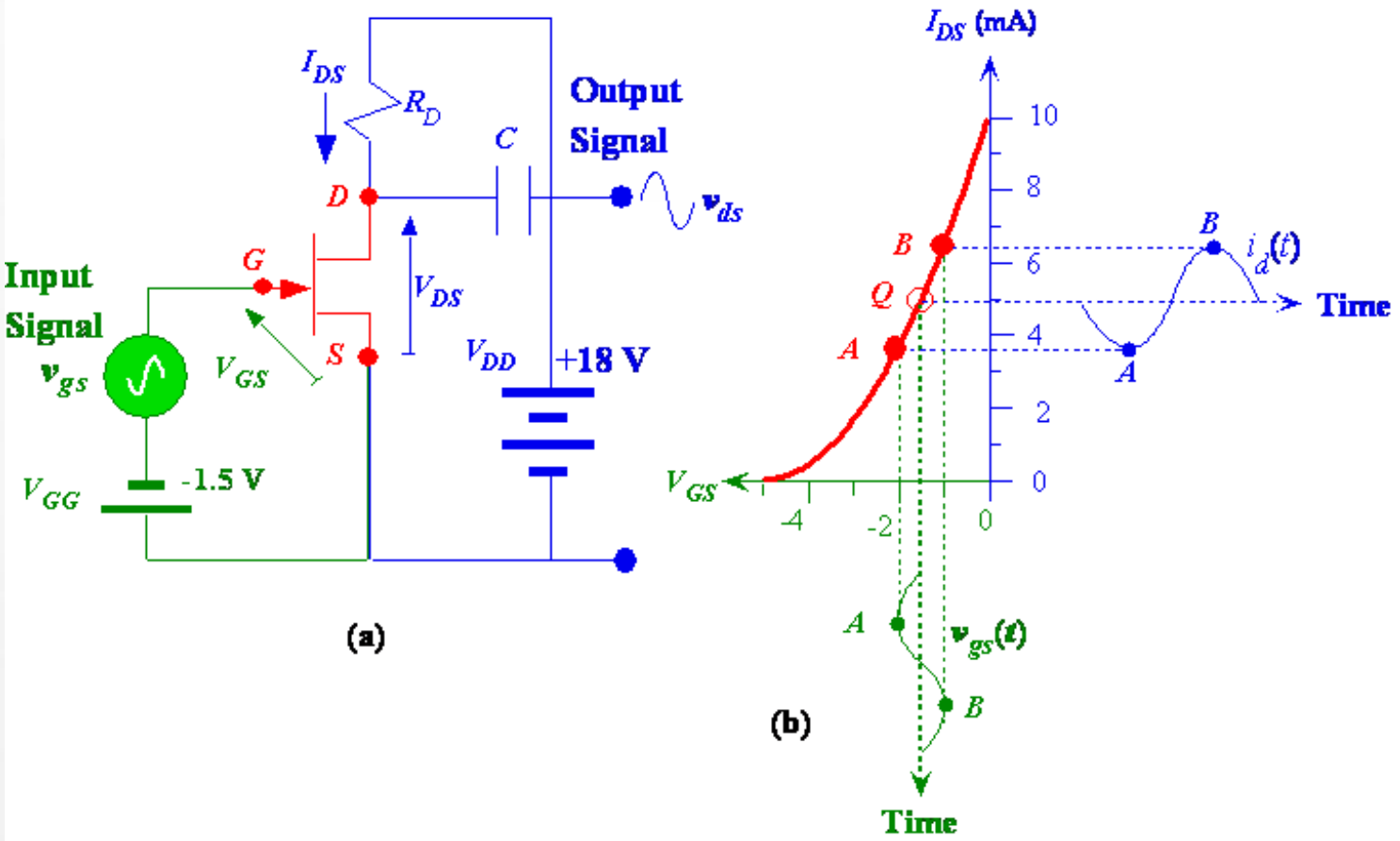
- THERE IS A CONVENIENT RELATIONSHIP BETWEEN I_{DS} AND V_{GS}.
- BEYOND PINCH-OFF

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS(off)}}\right)\right]^2$$

- WHERE I_{DSS} IS DRAIN CURRENT WHEN V_{GS}= 0 AND $V_{GS(OFF)}$ IS DEFINED AS $-V_P$, THAT IS GATE-SOURCE VOLTAGE THAT JUST PINCHES OFF THE CHANNEL.
- THE PINCH OFF VOLTAGE V_P HERE IS A +VE QUANTITY BECAUSE IT WAS INTRODUCED THROUGH $V_{DS(SAT)}$.
- $V_{GS(OFF)}$ HOWEVER IS NEGATIVE, $-V_P$.

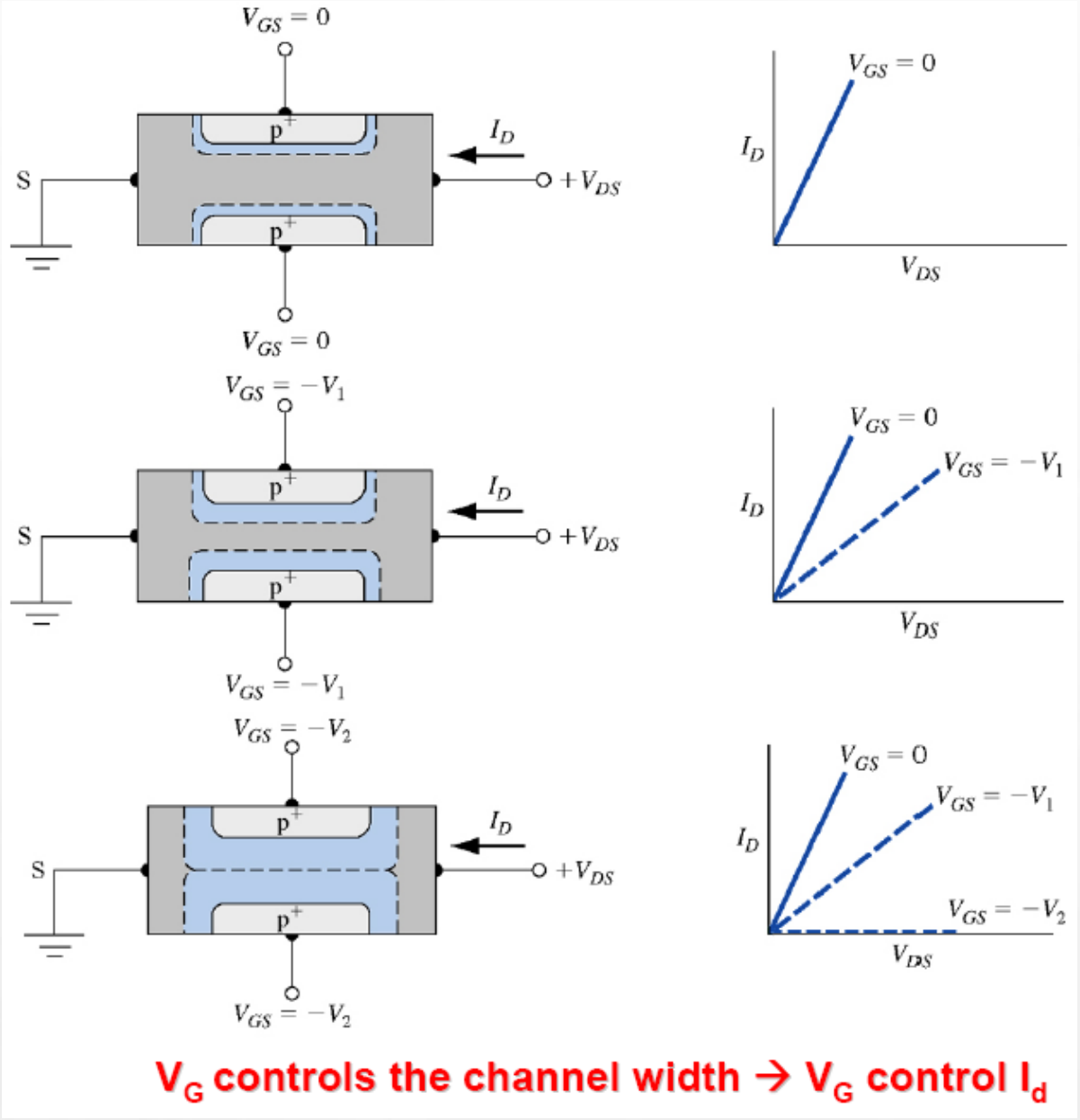


(a) Typical I_{DS} vs V_{GS} characteristics of a JFET (b).
The *DC* circuit in which V_{GS} in the gate-source circuit (input) controls the drain current I_{DS} in the drain-source (output) circuit in which V_{DS} is kept constant and large ($V_{DS} > V_P$).



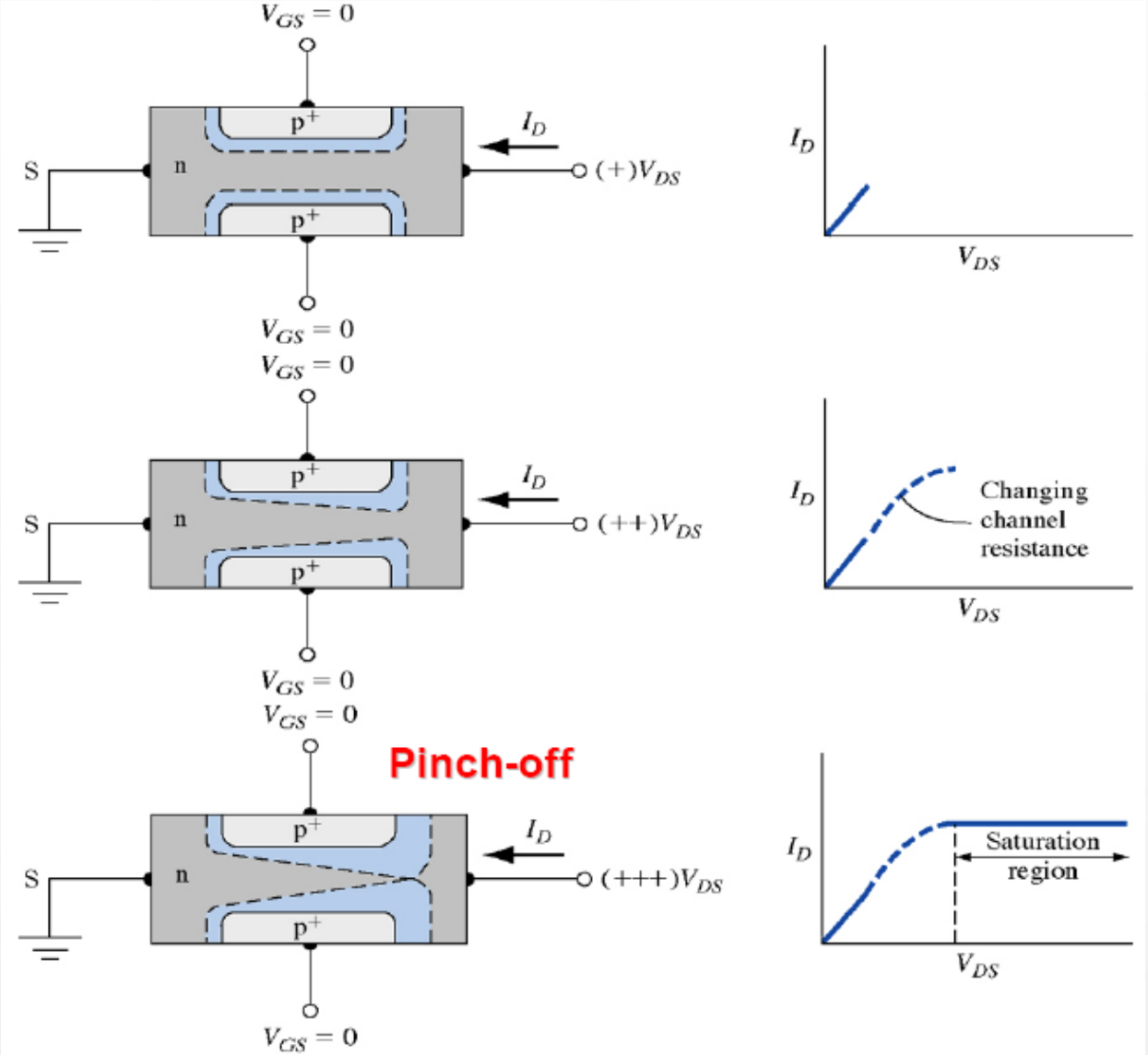
(a) Common source (CS) ac amplifier using a JFET.
(b) Explanation of how I_D is modulated by the signal v_{gs} in series with the dc bias voltage V_{GG}

I-V CHARACTERISTICS

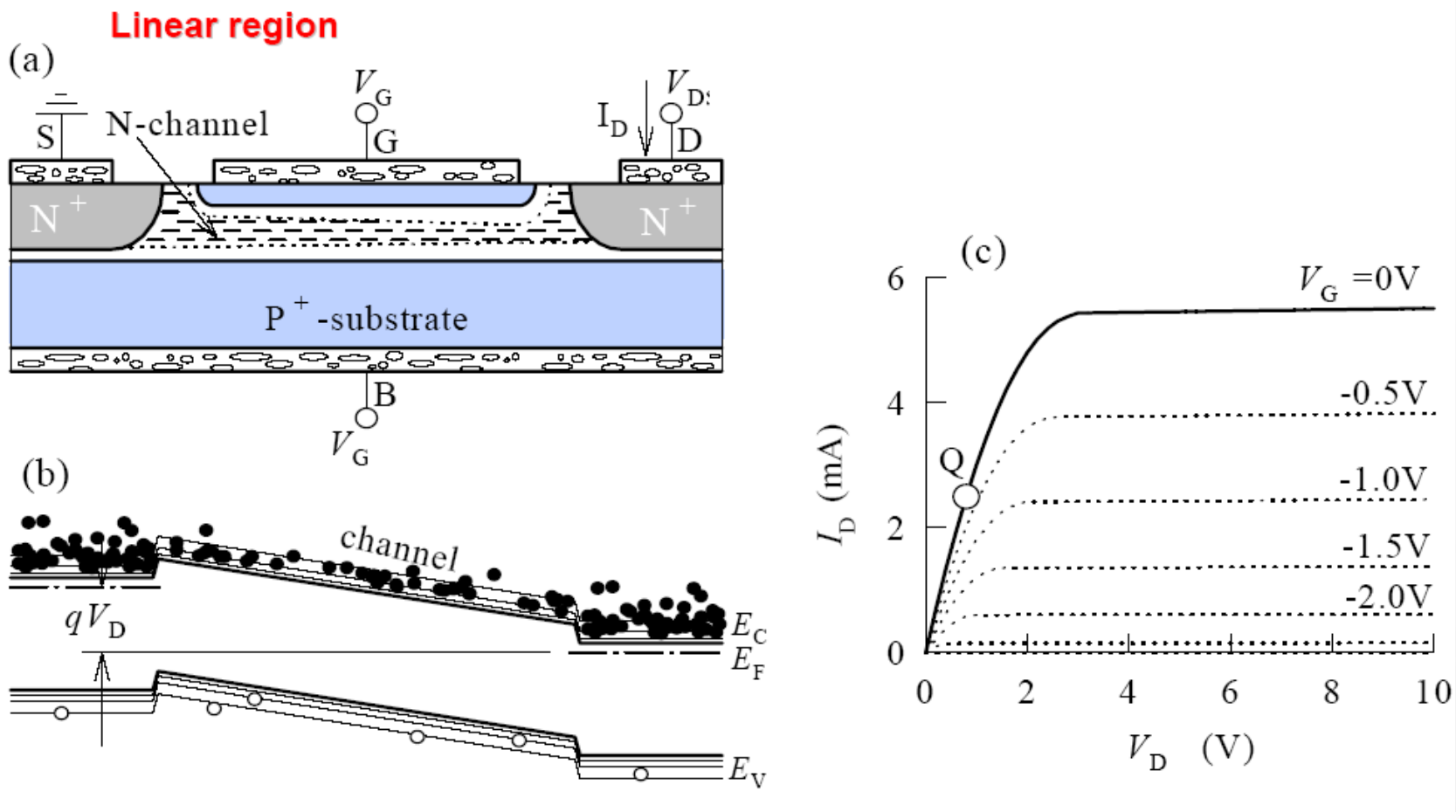


V_G controls the channel width → V_G control I_d

I-V CHARACTERISTICS



JFET: I-V CHARACTERISTICS



THE TRANSCONDUCTANCE CURVE

- THE PROCESS FOR PLOTTING TRANSCONDUCTANCE CURVE FOR A GIVEN JFET:
- PLOT A POINT THAT CORRESPONDS TO VALUE OF $V_{GS(OFF)}$.
- PLOT A POIT THAT CORRESPONDS TO VALUE OF I_{DSS}.
- SELECT 3 OR MORE VALUES OF V_{GS} BETWEEN 0 V AND $V_{GS(OFF)}$. FOR VALUE OF V_{GS}, DETERMINE THE CORRESPONDING VALUE OF I_D FROM

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- PLOT THE POINT FROM (3) AND CONNECT ALL THE PLOTTED POINT WITH A SMOOTH CURVE.

Example: Plot the transconductance curve for a JFET with $V_{GS(off)} = -6$ V and $I_{DSS} = 3$mA.

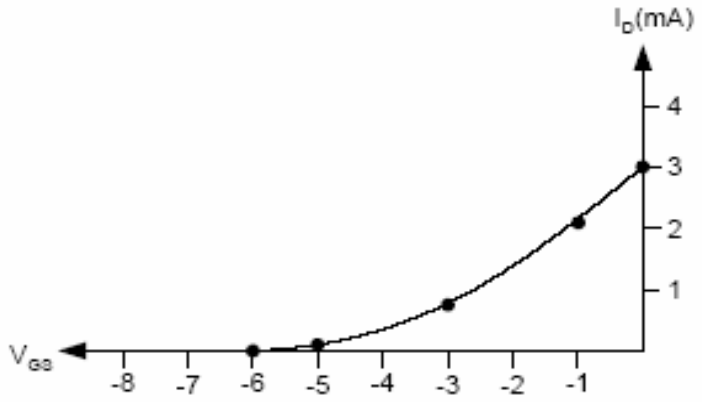
At $V_{GS(off)} = -6$ V , $I_D = 0$.

At $I_{DSS} = 3$ mA , $V_{GS} = 0$.

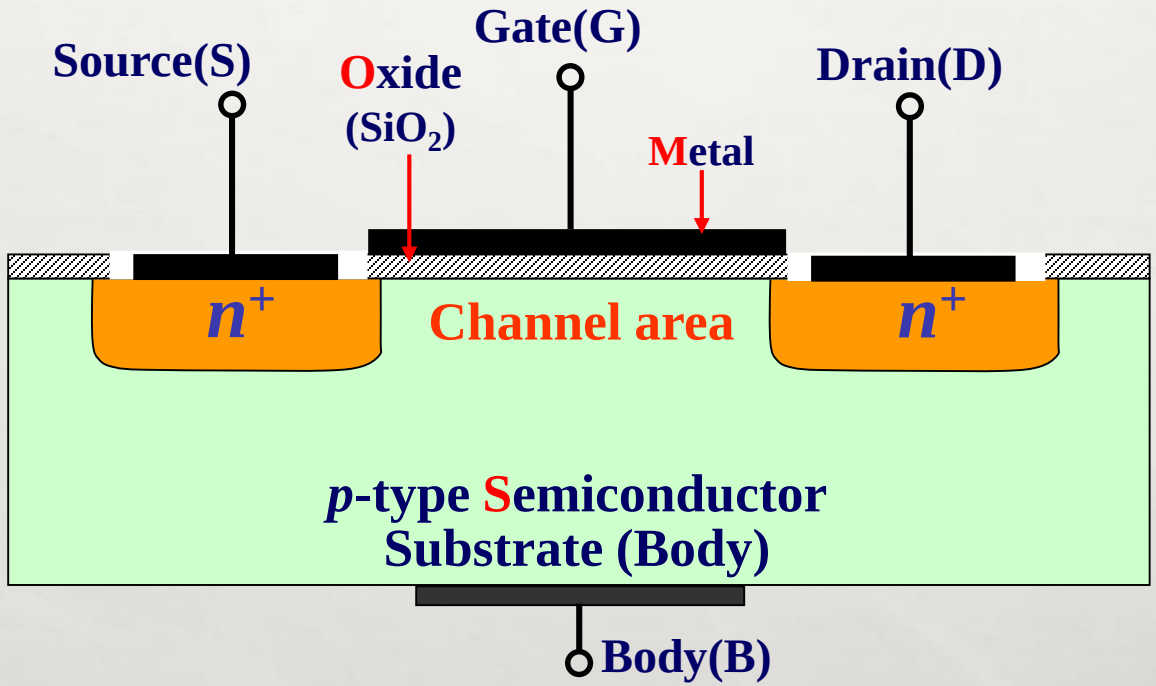
At $V_{GS} = -1$ V , $I_D = 2.08$ mA.

At $V_{GS} = -3$ V , $I_D = 0.75$ mA.

At $V_{GS} = -5$ V , $I_D = 0.083$ mA.

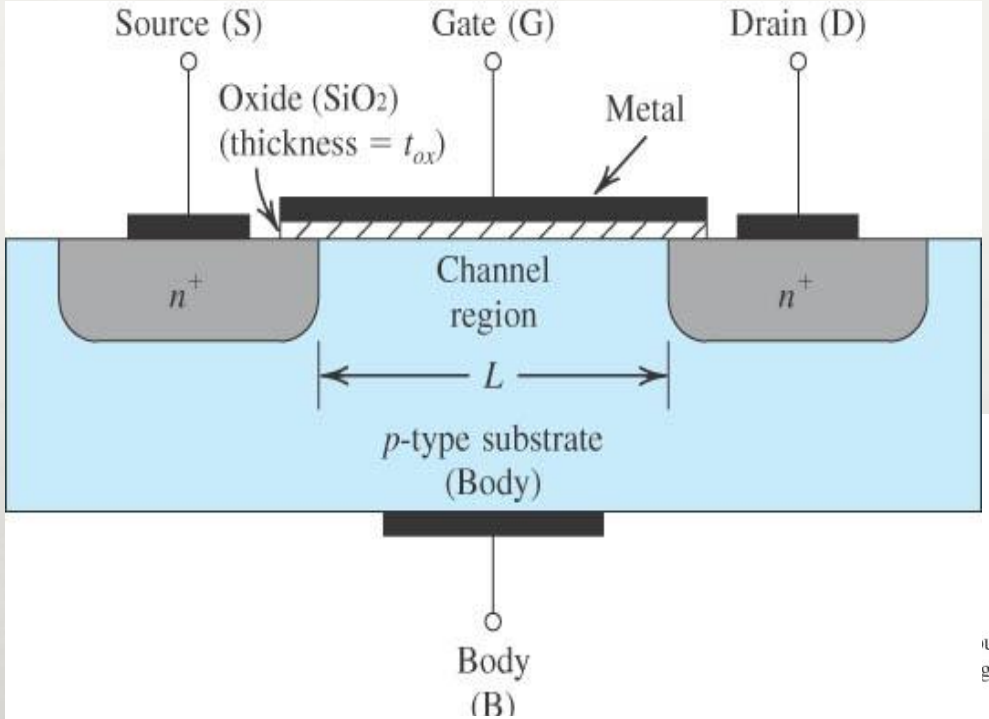


DEVICE STRUCTURE OF MOSFET (*N*-TYPE)



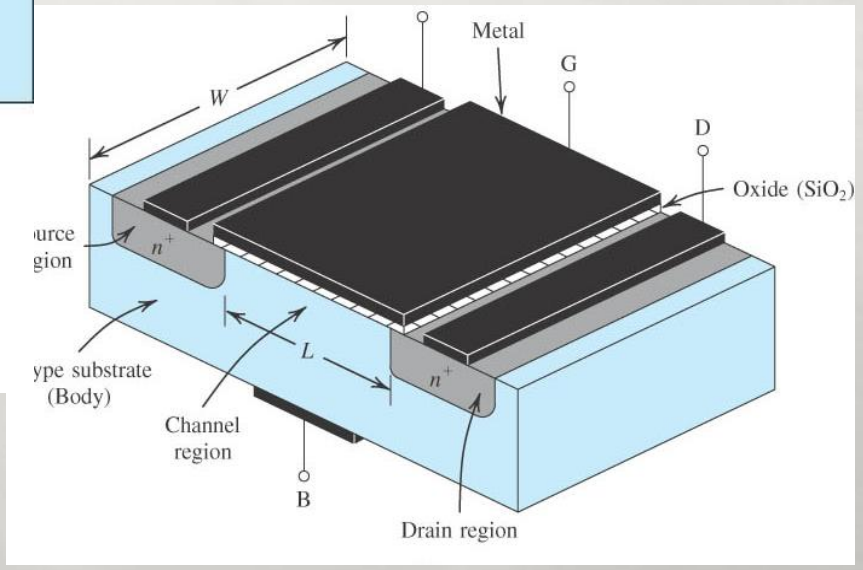
- **For normal operation, it is needed to create a conducting channel between Source and Drain**

DEVICE STRUCTURE OF MOSFET (*N*-TYPE)



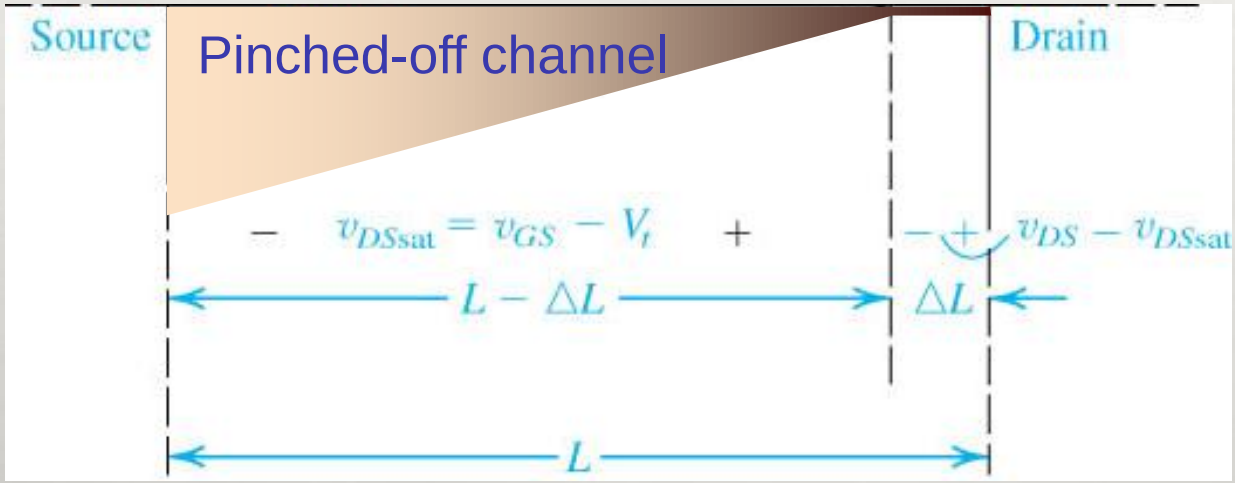
Cross-section view

- ***L* = 0.1 to 3 μm**
- ***W* = 0.2 to 100 μm**
- **T_{ox}= 2 to 50 nm**



DRAIN CURRENT UNDER PINCH OFF

- **The electrons pass through the pinch off area at very high speed so as the current continuity holds, similar to the water flow at the Yangtze Gorges**

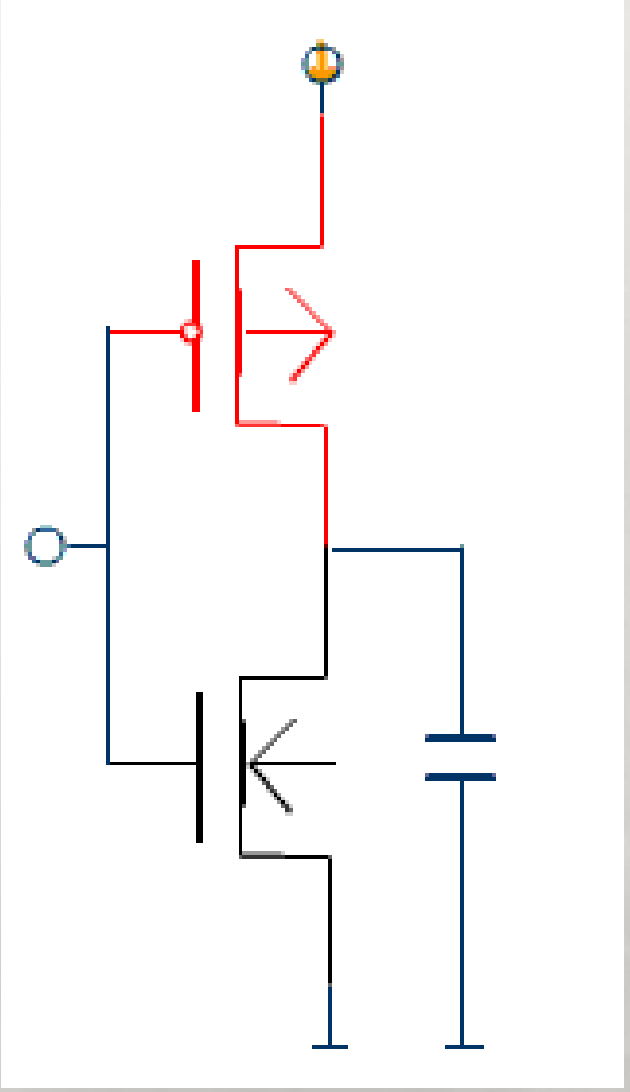


DRAIN CURRENT CONTROLLED BY V_{GS}

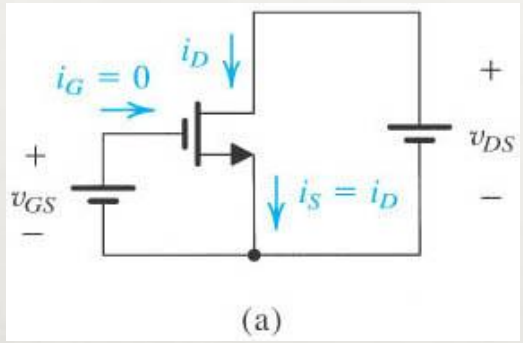
- V_{GS} CREATES THE CHANNEL.
- INCREASING V_{GS} WILL INCREASE THE CONDUCTANCE OF THE CHANNEL.
- AT SATURATION REGION ONLY THE V_{GS} CONTROLS THE DRAIN CURRENT.
- AT SUBTHRESHOLD REGION, DRAIN CURRENT HAS THE EXPONENTIAL RELATIONSHIP WITH V_{GS}

P CHANNEL DEVICE

- TWO REASONS FOR READERS TO BE FAMILIAR WITH *P* CHANNEL DEVICE
  - **Existence in discrete-circuit.**
  - **More important is the utilization of complementary MOS or CMOS circuits.**

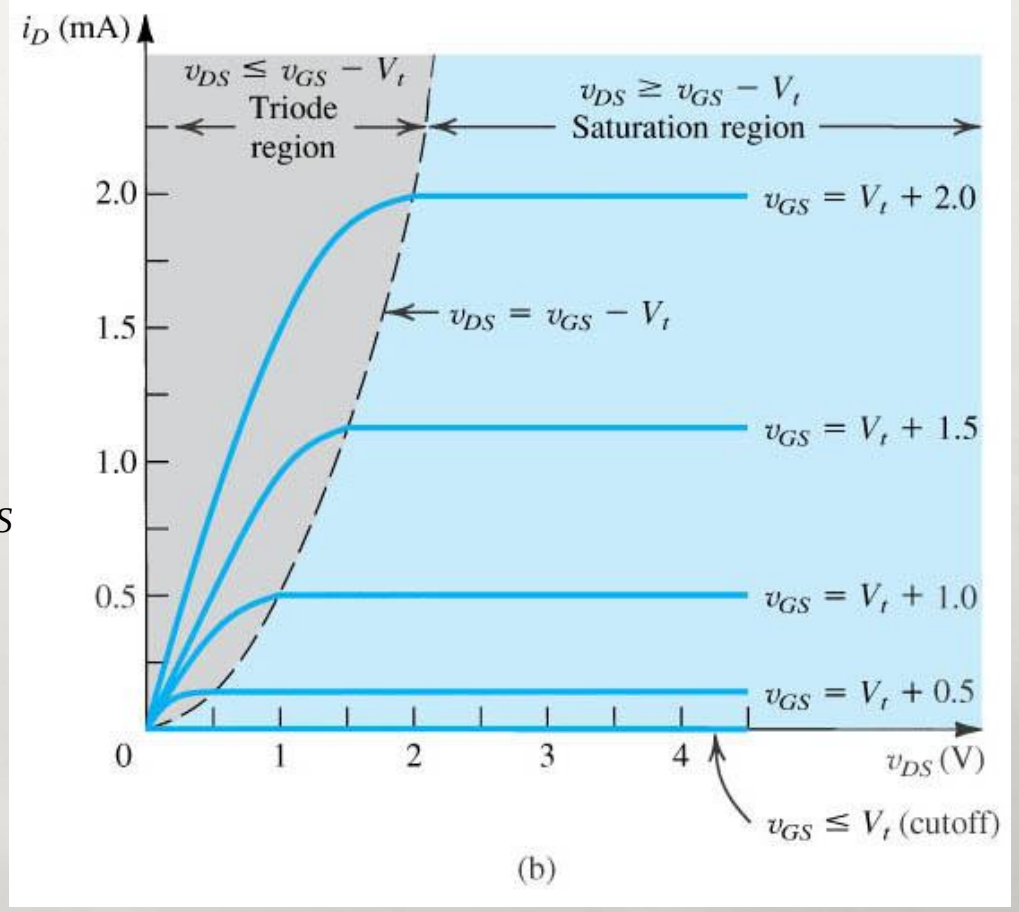


OUTPUT CHARACTERISTIC CURVES OF NMOS



(a) An *n*-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated.

(b) The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0$ mA/V^2.



OUTPUT CHARACTERISTIC CURVES OF NMOS

- Three distinct region
  - Cutoff region
  - Triode region
  - Saturation region
- Characteristic equations
- Circuit model

CUTOFF REGION

- Biased voltage

$$v_{GS} < V_t$$

- The transistor is turned off.

$$i_D = 0$$

- Operating in cutoff region as a switch.

TRIODE REGION

- Biased voltage

$$v_{GS} > V_t$$

$$v_{DS} < v_{GS} - V_t$$

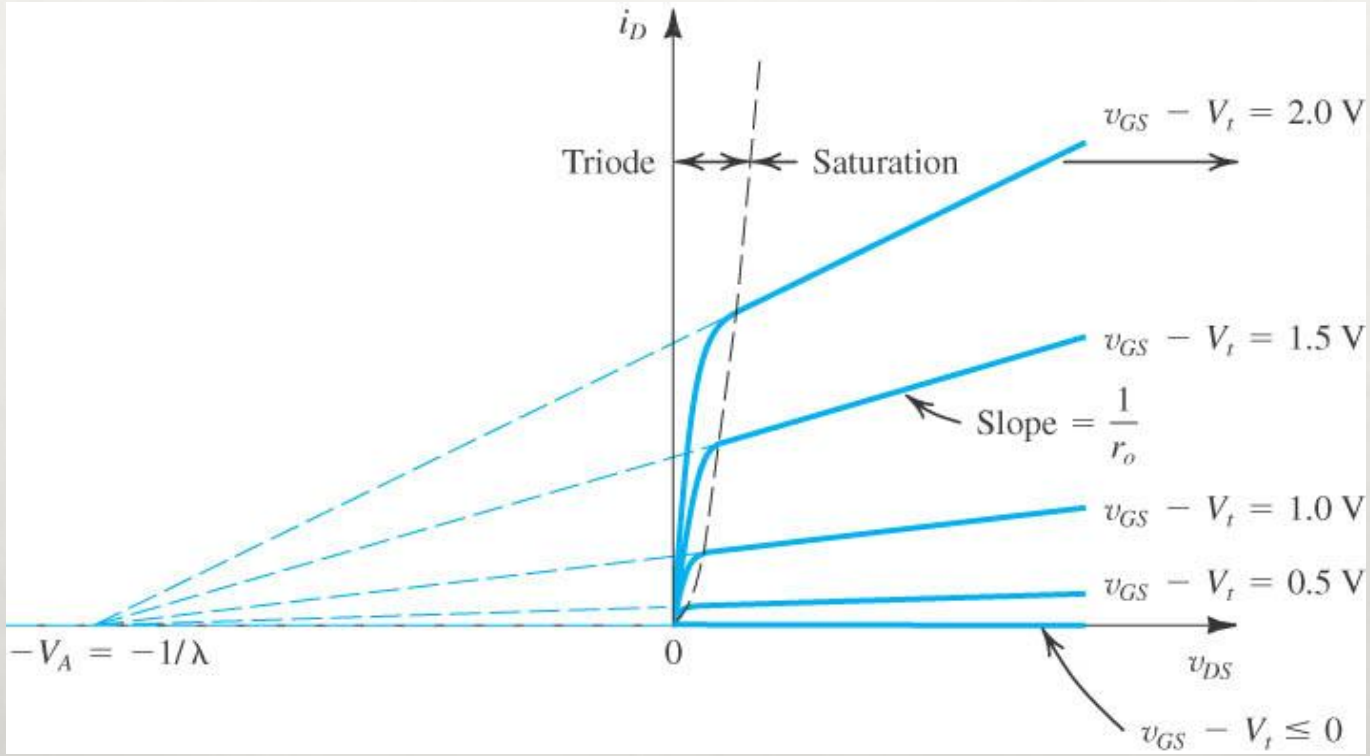
- The channel depth changes from uniform to tapered shape.
- Drain current is controlled not only by v_{DS} but also by v_{GS}

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}{v_{DS}}^2\right]$$

$$\approx k_n' \frac{W}{L}(v_{GS} - V_t)v_{DS}$$

process transcon-ductance parameter

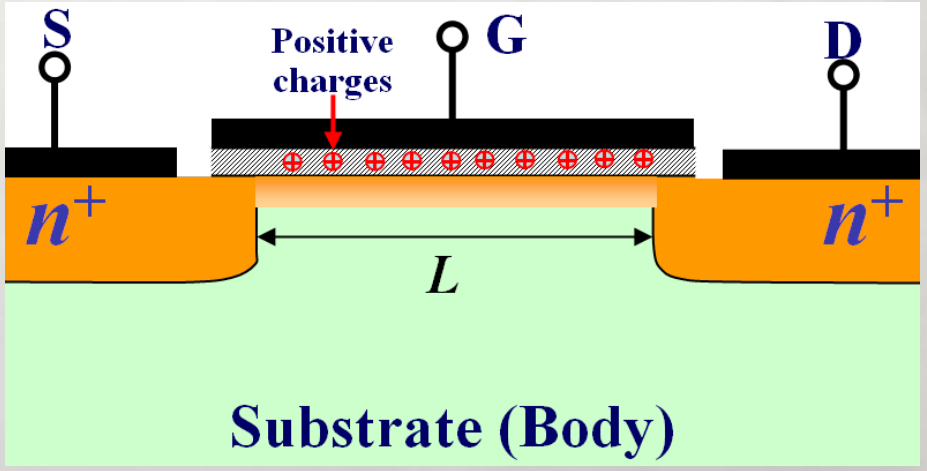
CHANNEL LENGTH MODULATION



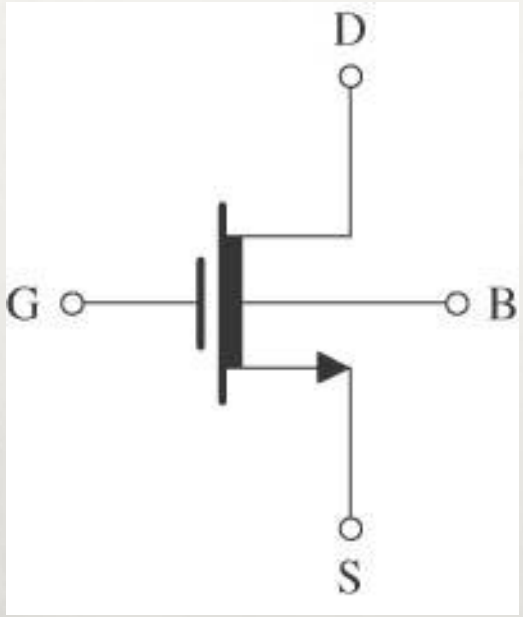
The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

THE DEPLETION-TYPE MOSFET

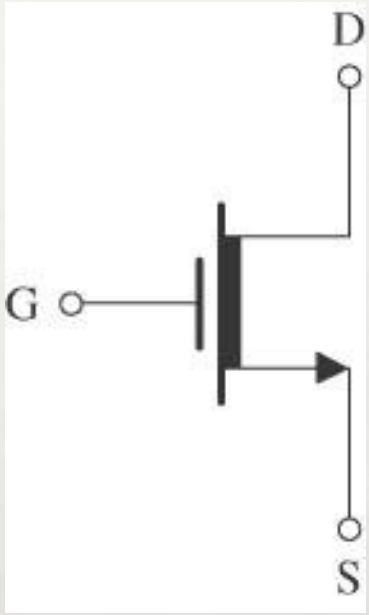
- PHYSICAL STRUCTURE
  - THE STRUCTURE OF DEPLETION-TYPE MOSFET IS SIMILAR TO THAT OF ENHANCEMENT-TYPE MOSFET WITH ONE IMPORTANT DIFFERENCE: *THE DEPLETION-TYPE MOSFET HAS A PHYSICALLY IMPLANTED CHANNEL*
    - **There is no need to induce a channel**
    - **The depletion MOSFET can be operated at both enhancement mode and depletion mode**



CIRCUIT SYMBOL FOR THE *N*-CHANNEL DEPLETION-MOS

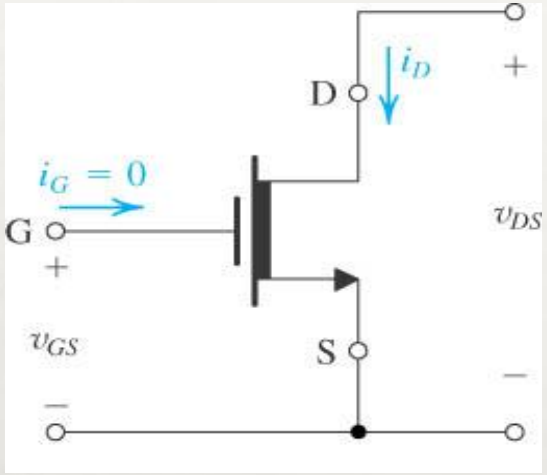


Circuit symbol for the *n*-channel depletion-type MOSFET



Simplified circuit symbol applicable for the case the substrate (B) is connected to the source (S).

CHARACTERISTIC CURVES

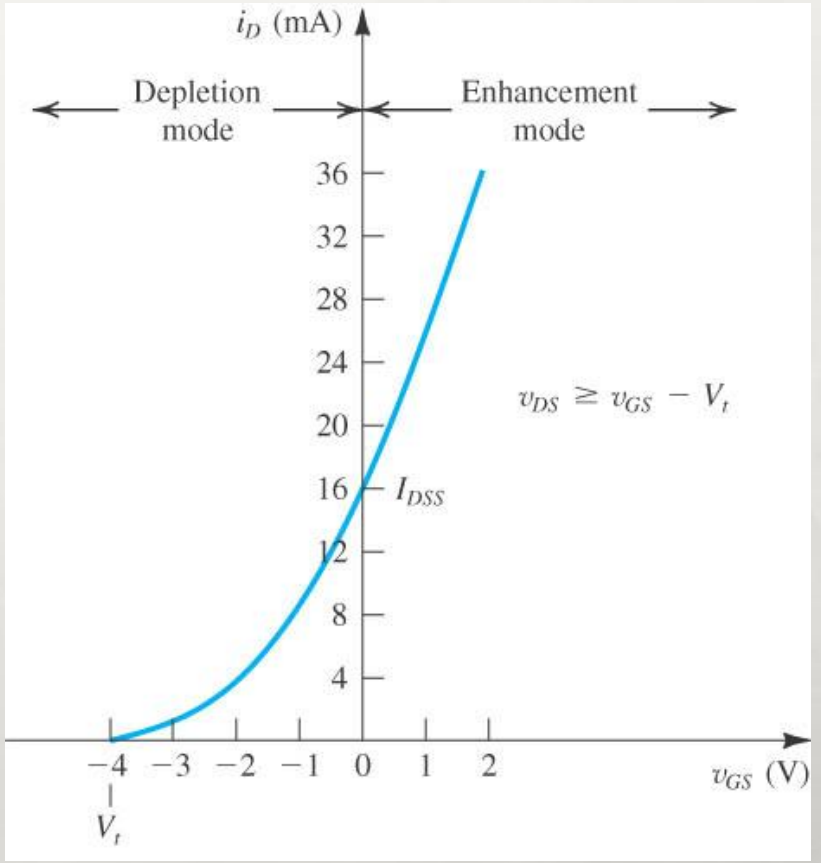


- Expression of characteristic equation

$$i_D = \tfrac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

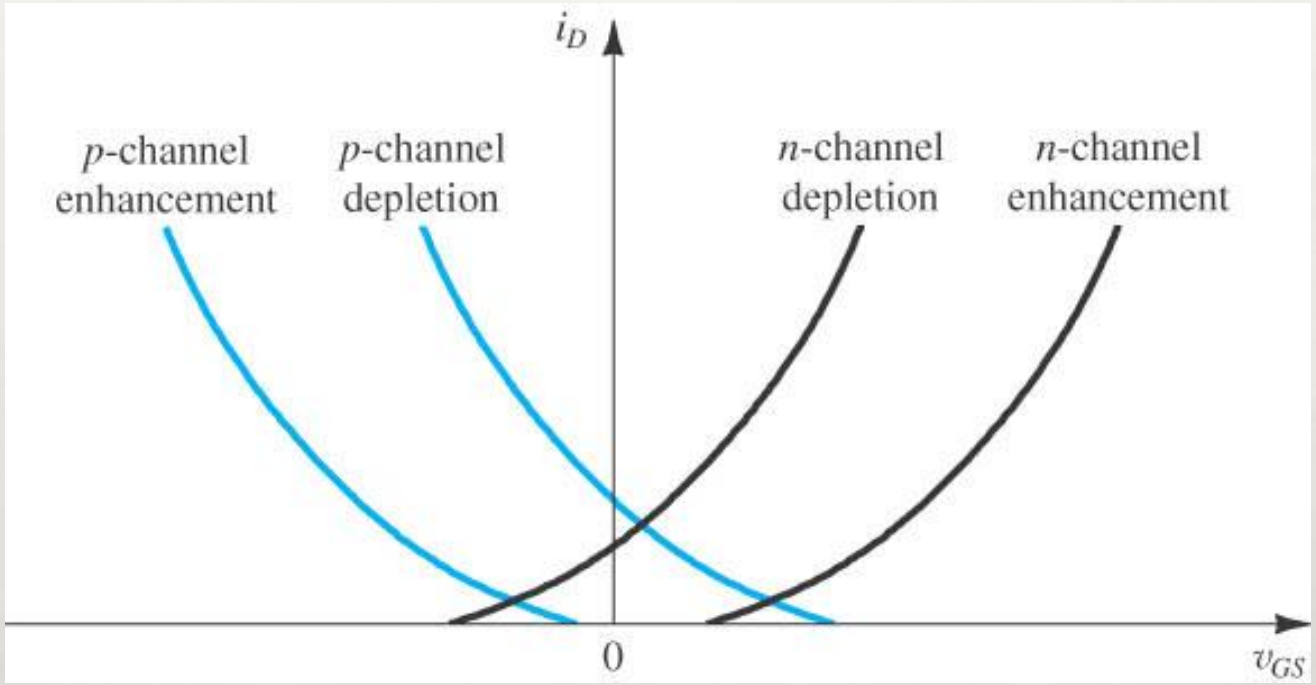
- Drain current with $v_{GS} = 0$

$$I_{DSS} = \tfrac{1}{2} k_n' \frac{W}{L} V_t^2$$



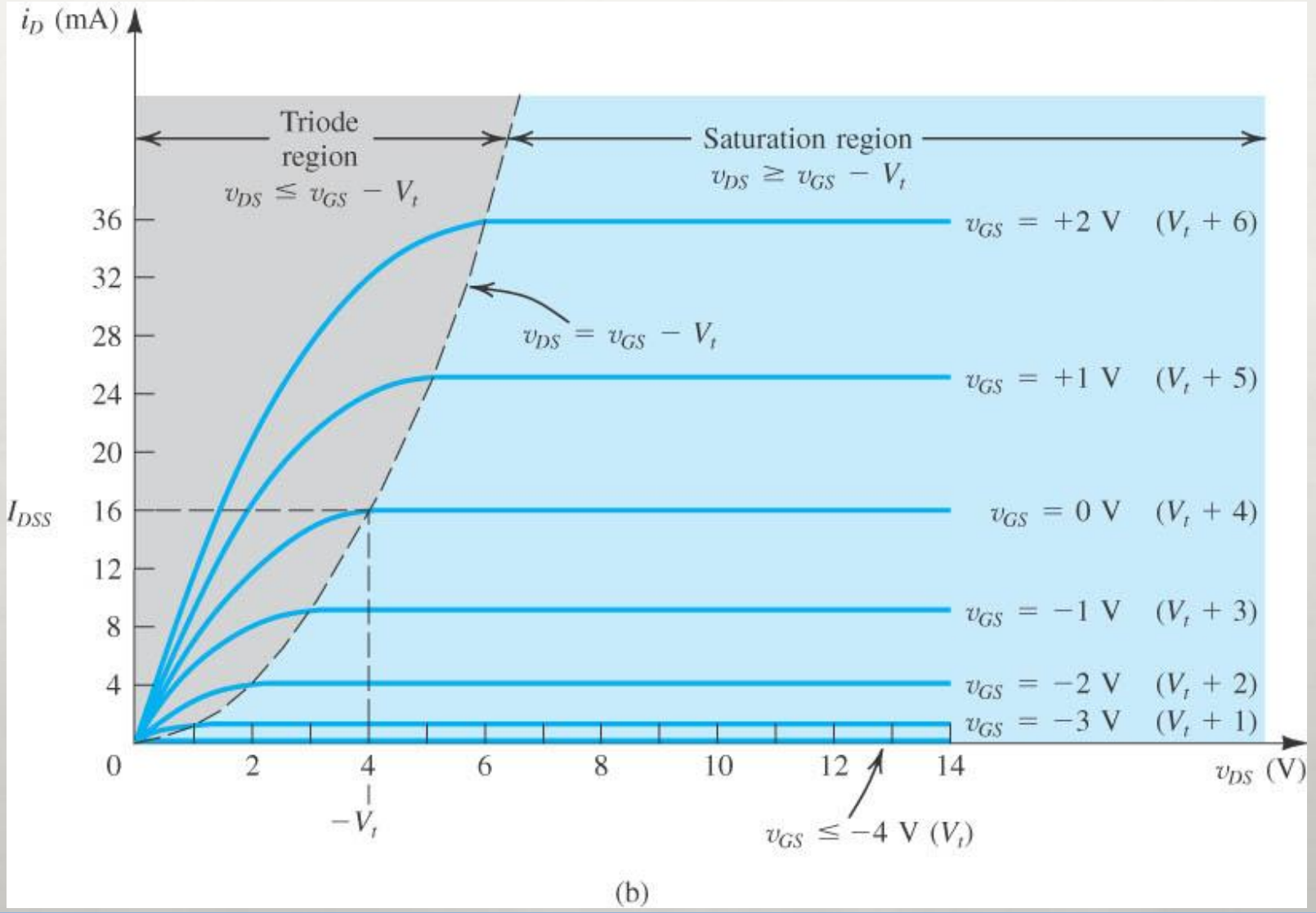
the i_D–v_{GS} characteristic in saturation

THE I_D–V_{GS} CHARACTERISTIC IN SATURATION



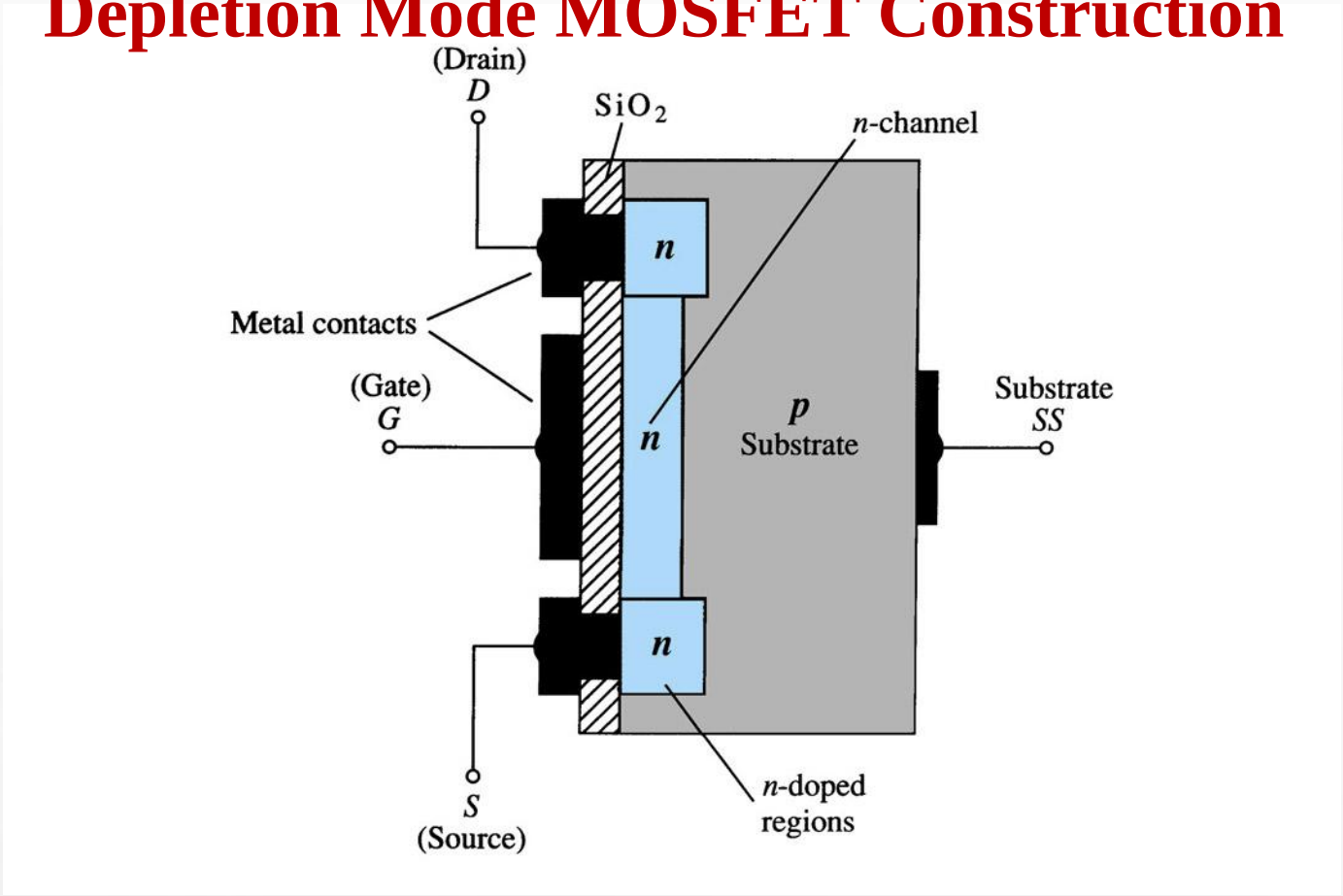
- Sketches of the i_D–v_{GS} characteristics for MOSFETs of enhancement and depletion types
- The characteristic curves intersect the v_{GS} axis at V_t.

THE OUTPUT CHARACTERISTIC CURVES



(b)

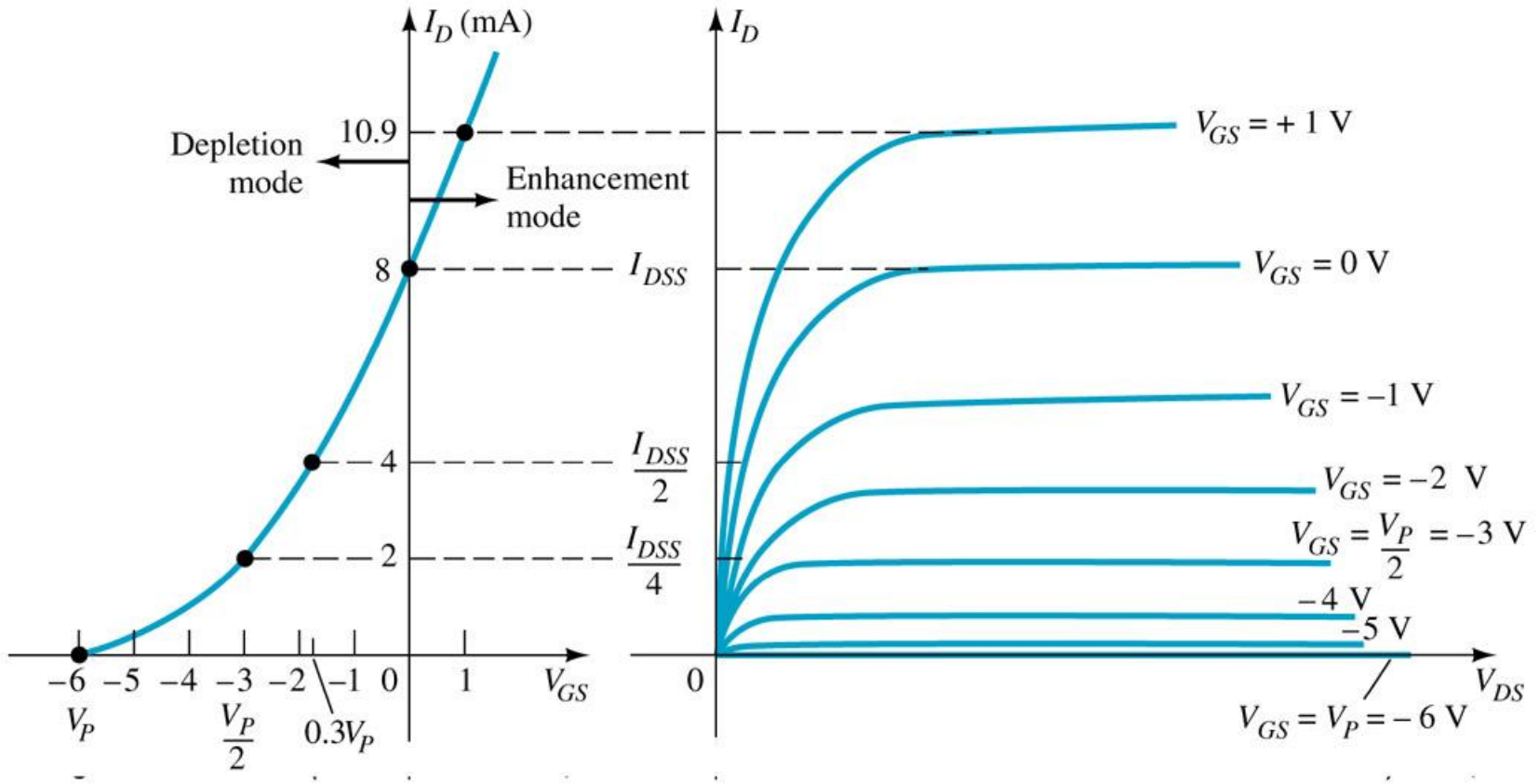
Depletion Mode MOSFET Construction



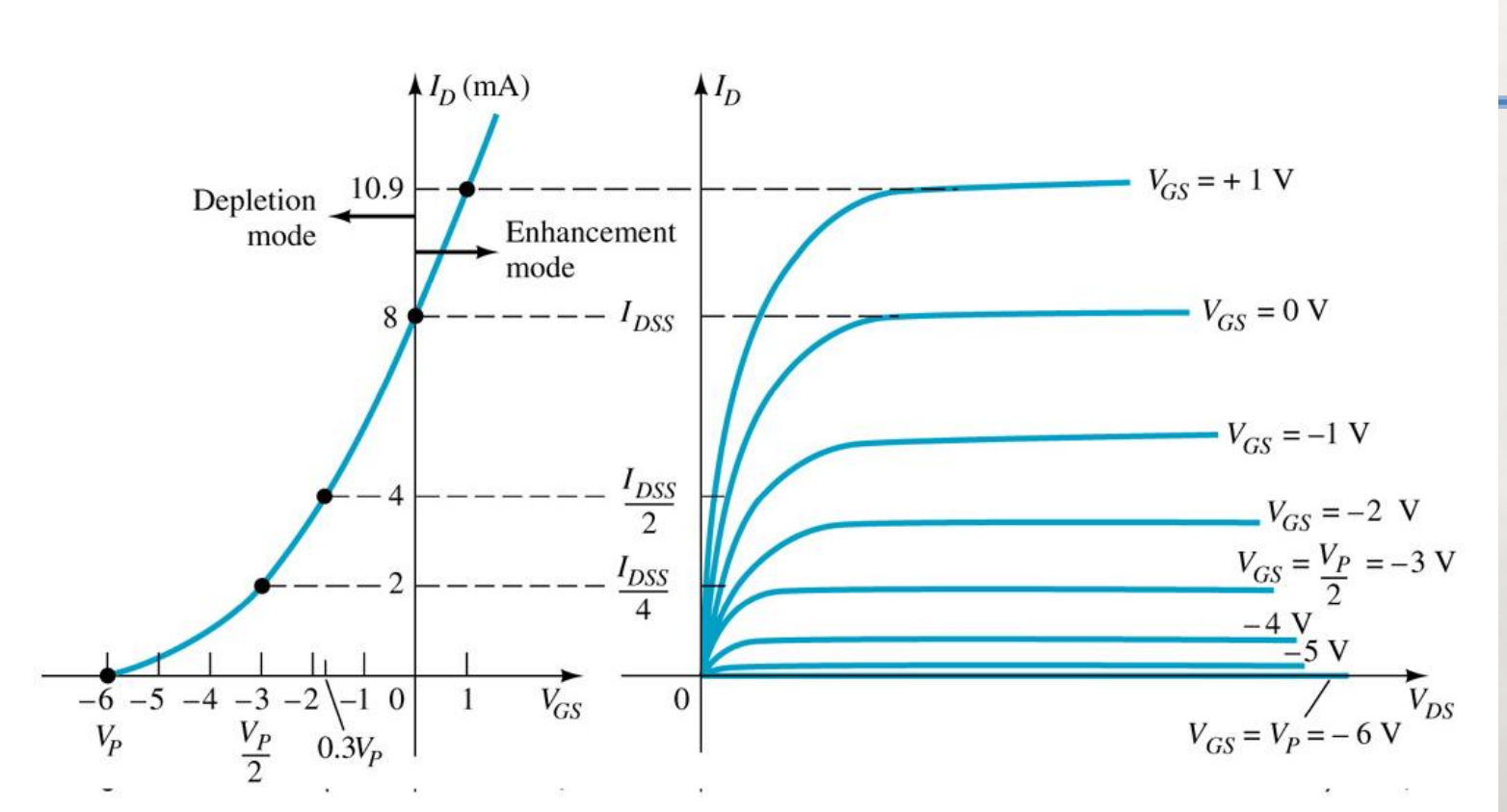
The Drain (D) and Source (S) leads connect to the to n-doped regions
These N-doped regions are connected via an n-channel
This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

OPERASI DASAR

A D-MOSFET may be biased to operate in two modes:
the **Depletion** mode or the **Enhancement** mode



D-MOSFET DEPLETION MODE OPERATION



The transfer characteristics are similar to the JFET

In Depletion Mode operation:

When $V_{GS} = 0V$, $I_D = I_{DSS}$

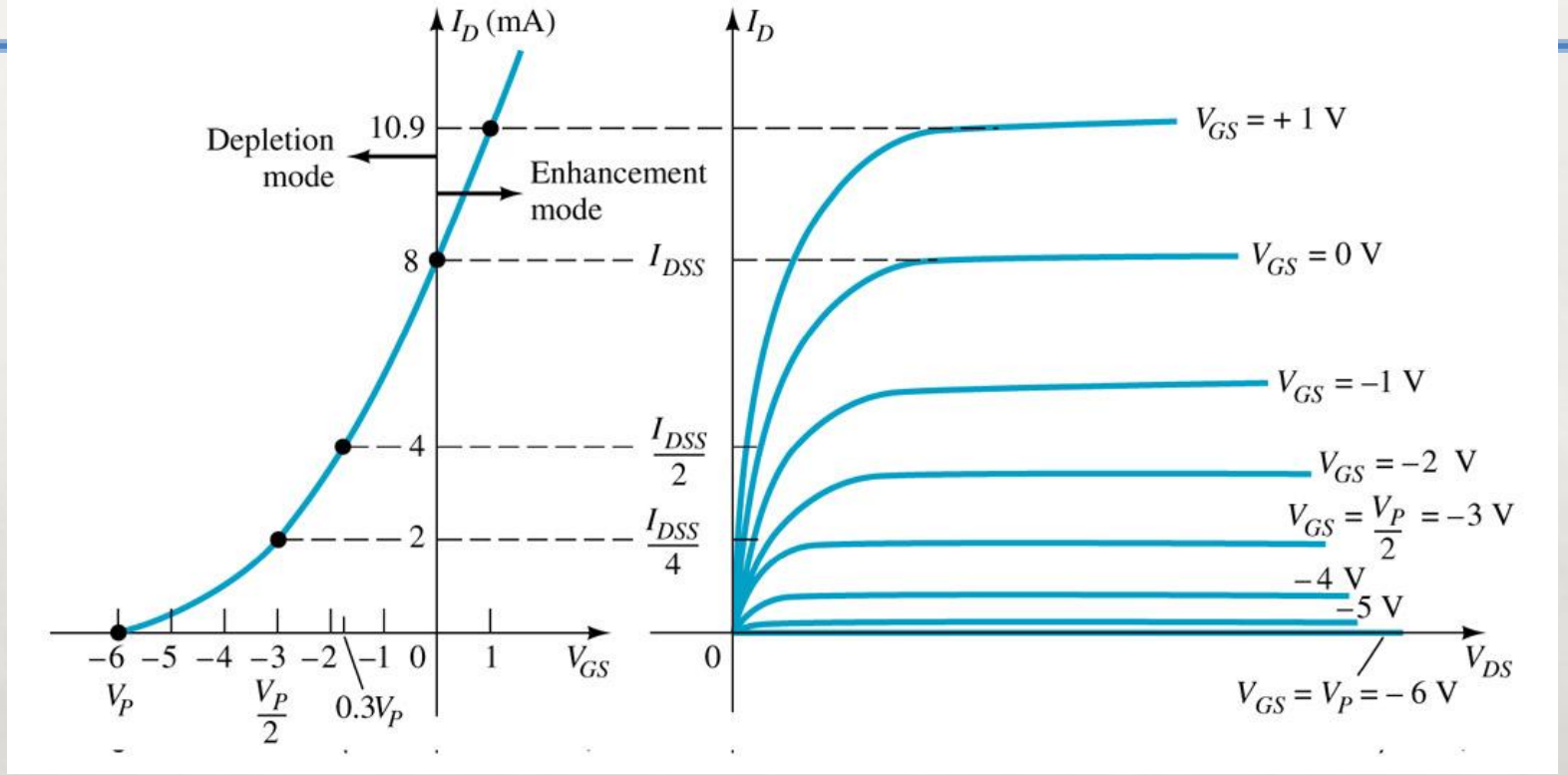
When $V_{GS} < 0V$, $I_D < I_{DSS}$

When $V_{GS} > 0V$, $I_D > I_{DSS}$

The formula used to plot the Transfer Curve, is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

D-MOSFET ENHANCEMENT MODE OPERATION



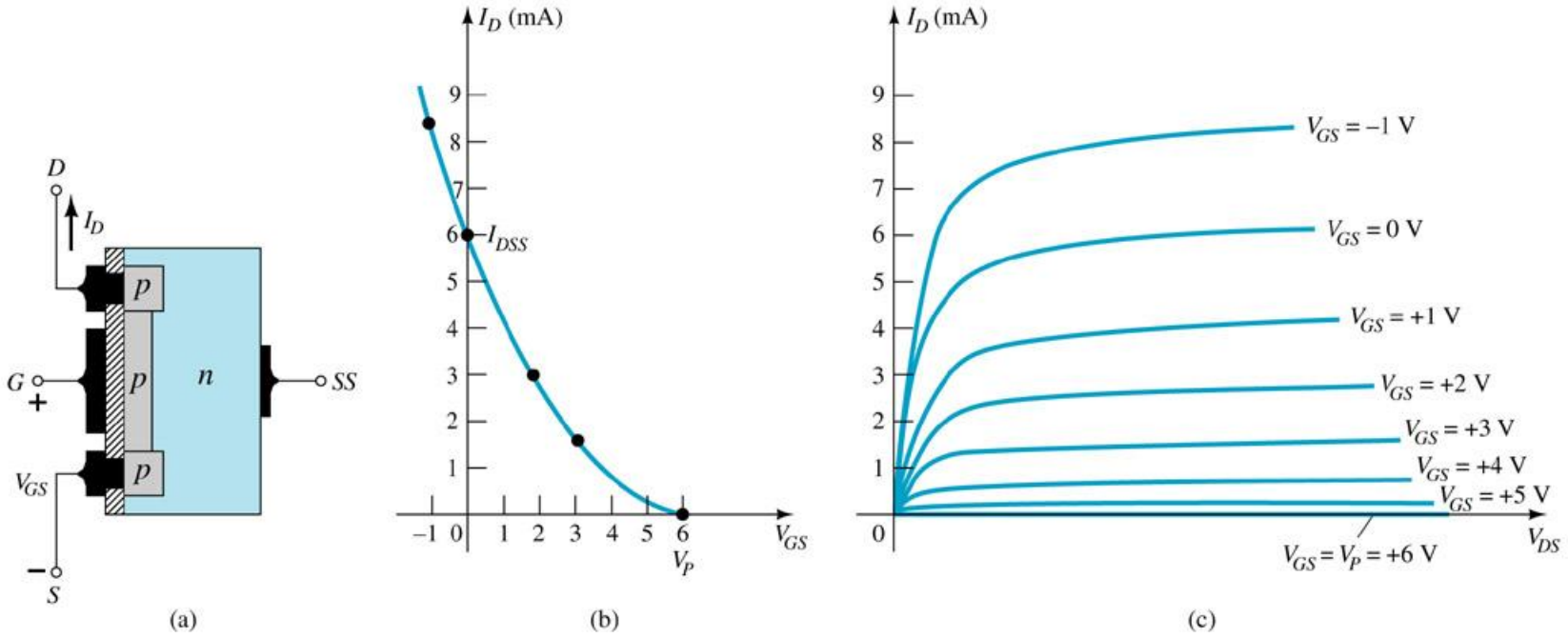
Enhancement Mode operation

In this mode, the transistor operates with $V_{GS} > 0V$, and I_D increases above I_{DSS}

Shockley's equation, the formula used to plot the Transfer Curve, still applies but V_{GS} is positive:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

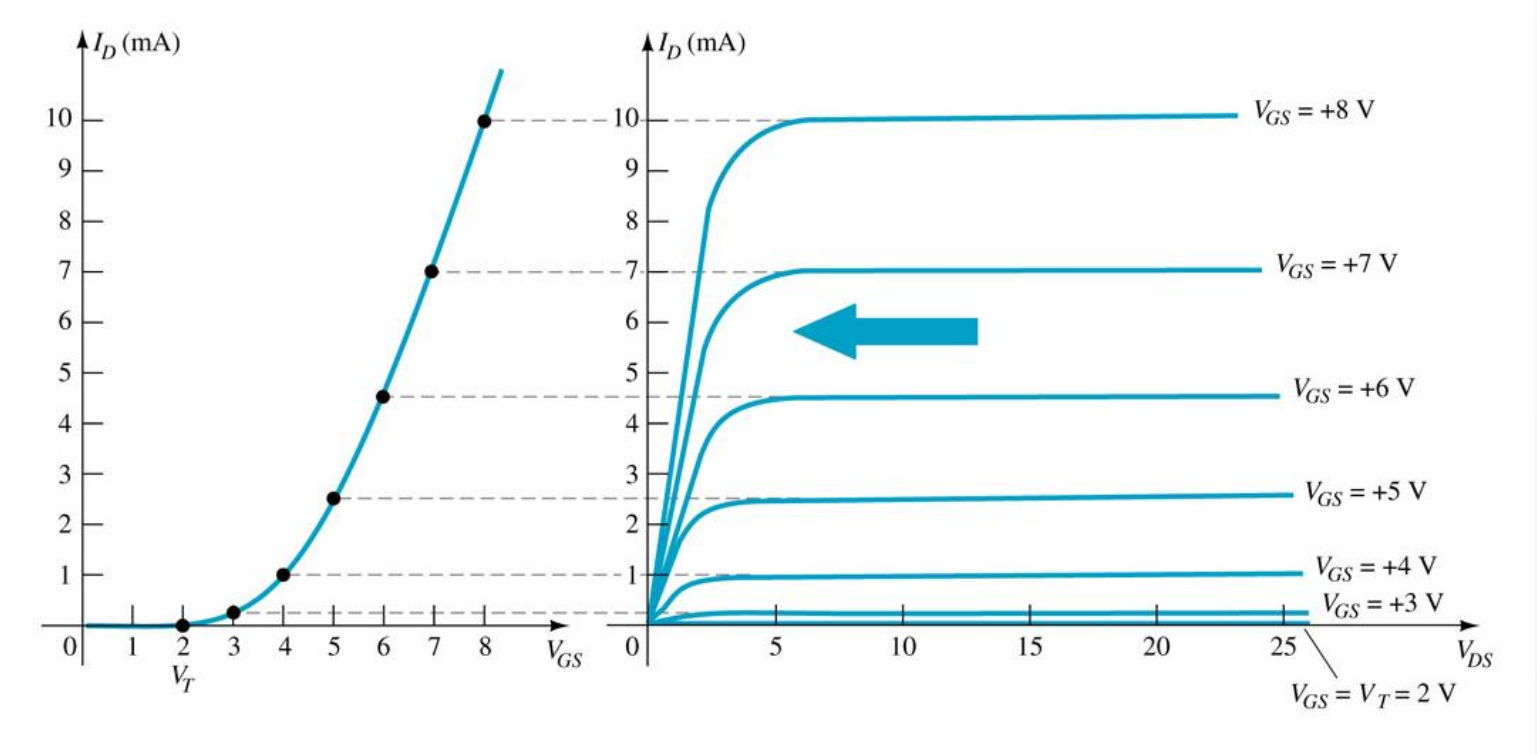
p-Channel Depletion Mode MOSFET



The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed

Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive

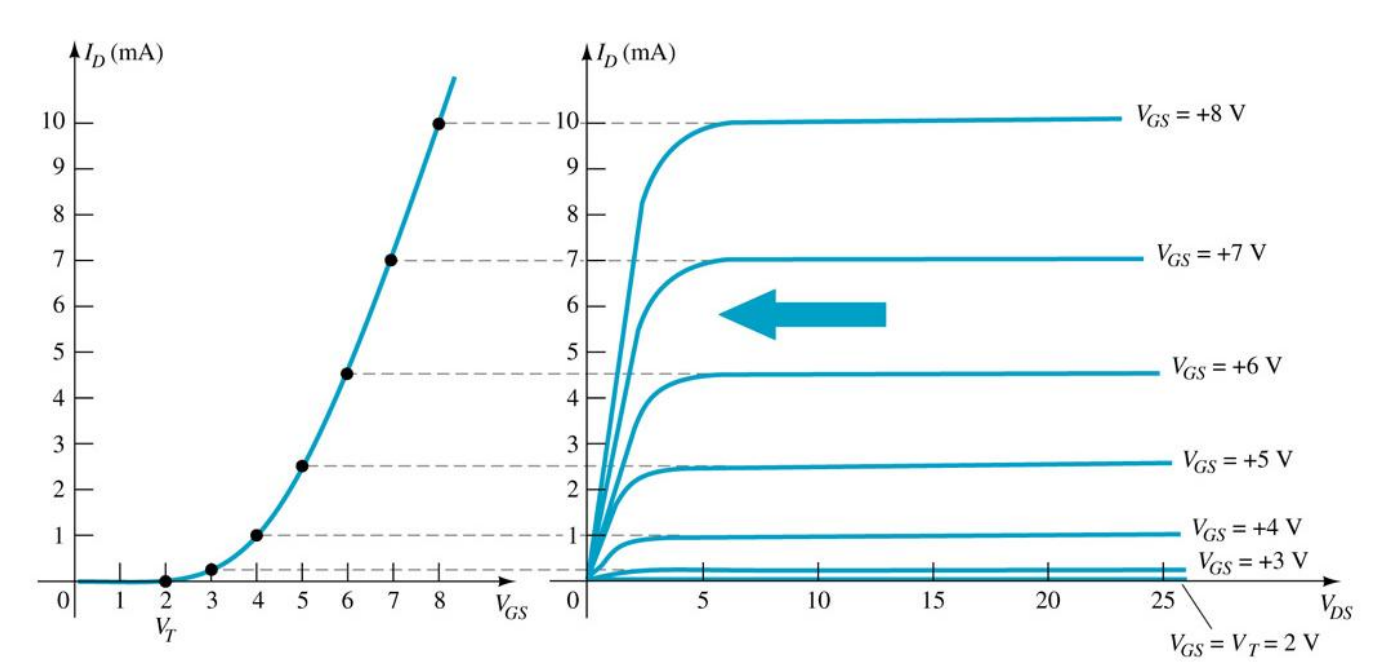
$I_{DSS} = 0$ when $V_{GS} < V_T$

As V_{GS} increases above V_T, I_D increases

If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})

The saturation level, V_{DSsat} is reached.

TRANSFER CURVE



To determine I_D given V_{GS}: $\mathbf{I_D = k\,(V_{GS} - V_T)^2}$ $\qquad \mathbf{k = \dfrac{I_{D(on)}}{(V_{GS(ON)} - V_T)^2}}$

where V_T = threshold voltage or voltage at which the MOSFET turns on.

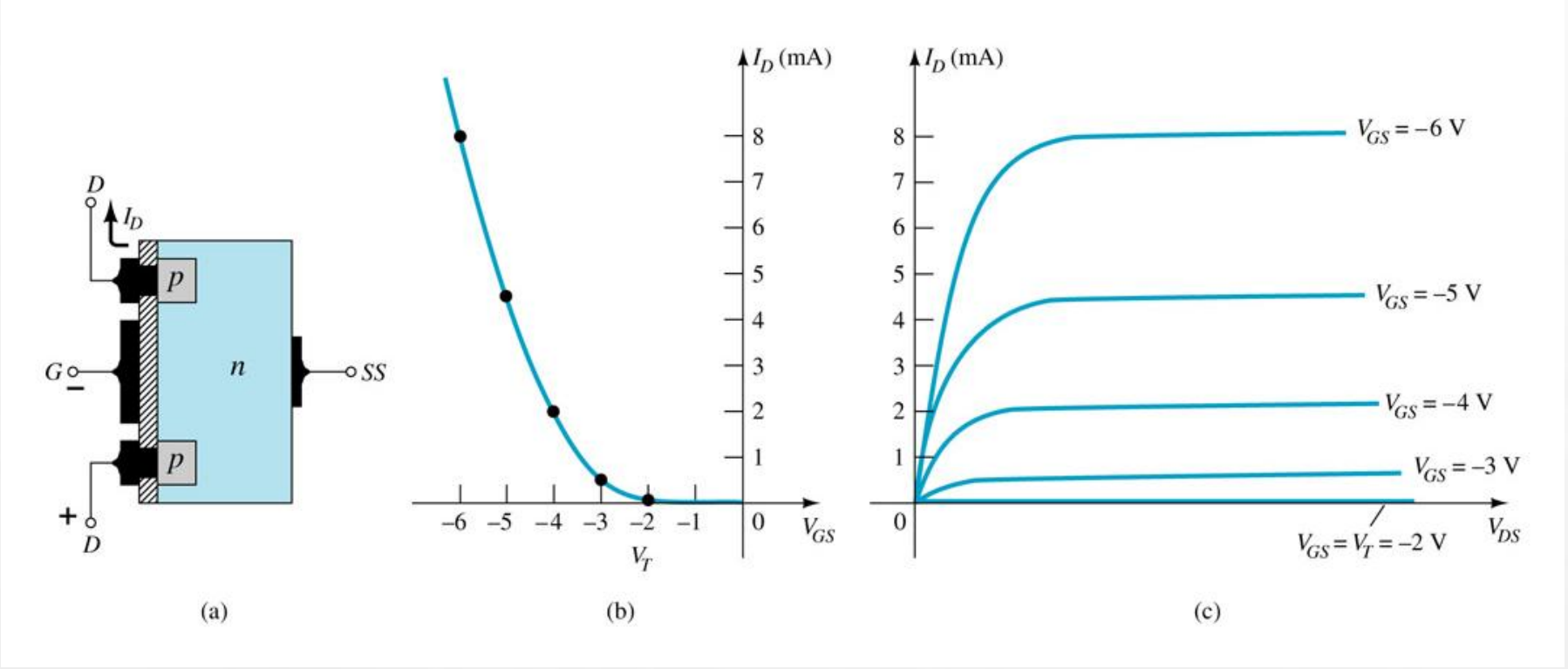
k = constant found in the specification sheet

The PSpice determination of k is based on the geometry of the device:

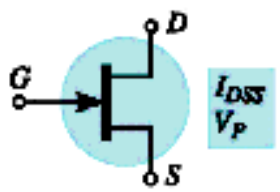
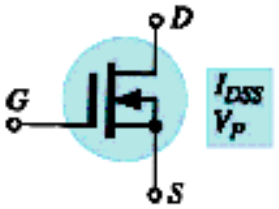
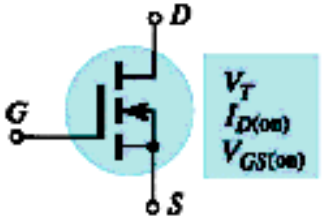
$$\mathbf{k = \left(\frac{W}{L}\right)\left(\frac{KP}{2}\right)} \qquad \textbf{where } \mathbf{KP = \mu_N C_{OX}}$$

P-CHANNEL ENHANCEMENT MODE MOSFETS

The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



Tabel Rangkuman

JFET	D-MOSFET	E-MOSFET
$I_G = 0\ \text{A}, I_D = I_S$	$I_G = 0\ \text{A}, I_D = I_S$	$I_G = 0\ \text{A}, I_D = I_S$
		
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$I_D = k(\ _{GS} - V_{GS(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$