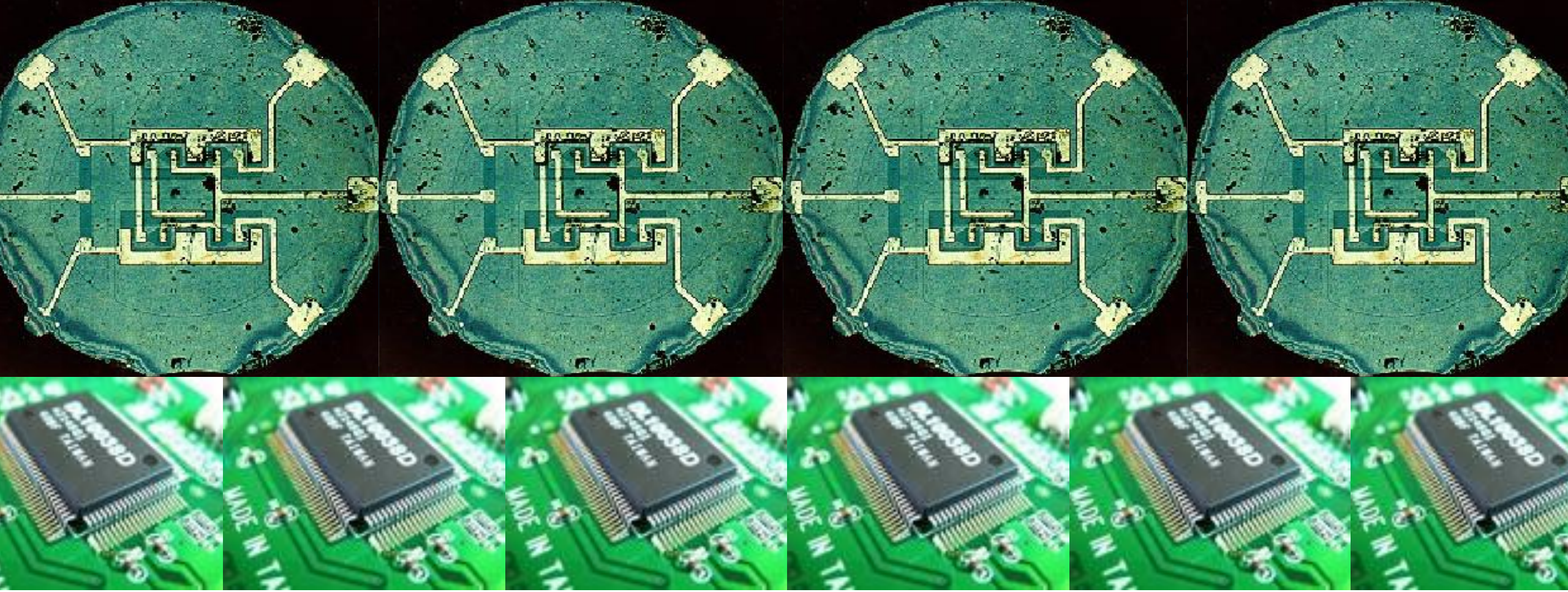


PENGENALAN TEKNOLOGI TERINTEGRASI

Eka Maulana, ST, MT, MEng.
Universitas Brawijaya

PENGANTAR: TREND PERKEMBANGAN PROSESOR

Brand	Desktop				Mobile			
	Code-named	Cores	Fab	Date released	Code-named	Cores	Fab	Date released
Core 2 Duo	Conroe	2	65 nm	August 2006	Merom	2	65 nm	July 2006
	Allendale	2	65 nm	January 2007	Penryn	2	45 nm	January 2008
	Wolfdale	2	45 nm	January 2008				
Core i7	Bloomfield	4	45 nm	November 2008				
	Lynnfield	4	45 nm	September 2009	Clarksfield	4	45 nm	September 2009
	Gulftown	6	32 nm	July 2010	Arrandale	2	32 nm	January 2010
	Sandy Bridge	4	32 nm	January 2011	Sandy Bridge	4	32 nm	January 2011
	Sandy Bridge-E	6	32 nm	November 2011	Sandy Bridge	2	32 nm	February 2011
	Sandy Bridge-E	4	32 nm	February 2012	Ivy Bridge	4	22 nm	May 2012
	Ivy Bridge	4	22 nm	April 2012	Ivy Bridge	2	22 nm	May 2012
	Haswell	4	22 nm	June 2013	Haswell	4	22 nm	June 2013
	Ivy Bridge-E	4	22 nm	September 2013	Haswell	2	22 nm	June 2013
	Ivy Bridge-E	6	22 nm	September 2013				
	Haswell-E	6	22 nm	August 2014				
Core i7 Extreme Edition	Bloomfield	4	45 nm	November 2008	Clarksfield	4	45 nm	September 2009
	Gulftown	6	32 nm	March 2010	Sandy Bridge	4	32 nm	January 2011
	Sandy Bridge-E	6	32 nm	November 2011	Ivy Bridge	4	22 nm	May 2012
	Ivy Bridge-E	6	22 nm	September 2013	Haswell	4	22 nm	June 2013
	Haswell-E	8	22 nm	August 2014				

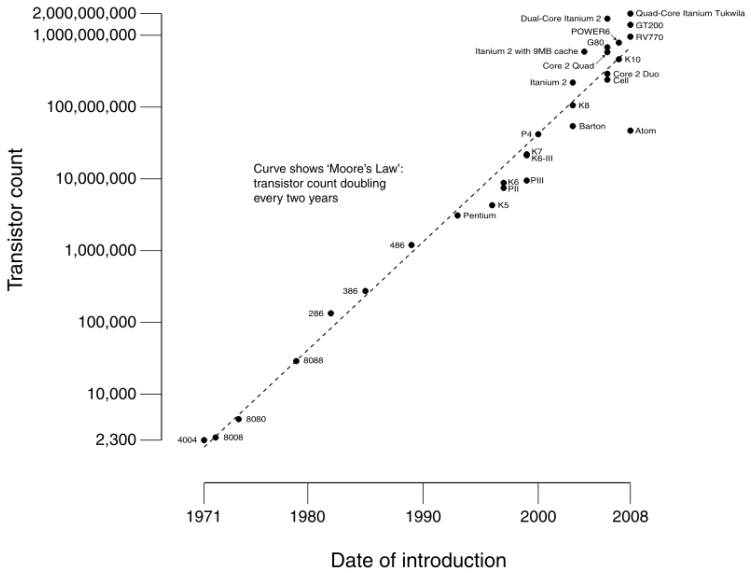
PERKEMBANGAN PROSESOR

Brand Name & Processor Number[1]	Base Clock Speed (GHz)	Turbo Frequency[2] (GHz)	Cores/ Threads	Cache	Memory Support	TDP	Socket (LGA)	Pricing (1k USD)
NEW Intel® Core™ i7 4960X Unlocked	3.6	Up to 4.0	6/12	15 MB	4 channels DDR3 1866	130W	2011	$990
NEW Intel® Core™ i7 4930K Unlocked	3.4	Up to 3.9	6/12	12 MB	4 channels DDR3 1866	130W	2011	$555
NEW Intel® Core™ i7 4820K Unlocked	3.7	Up to 3.9	4/8	10 MB	4 channels DDR3 1866	130W	2011	$310
Intel® Core™ i7-4770K Unlocked	3.5	Up to 3.9	4/8	8 MB	2 channels DDR3 1600	95W	1150	$317

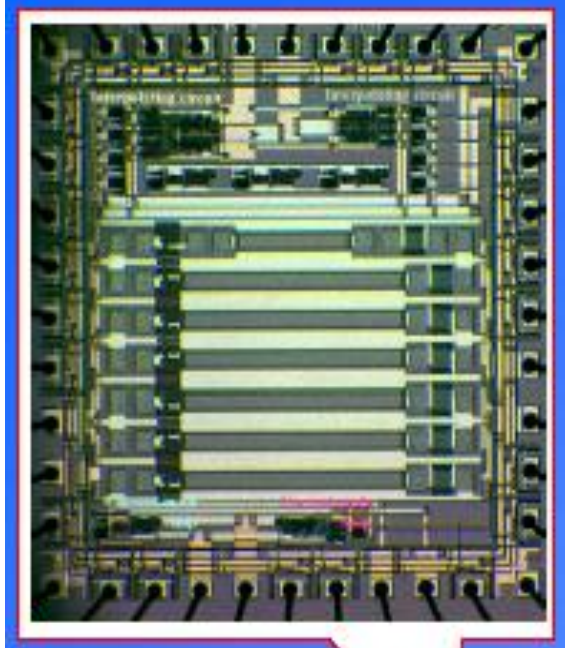
JUMLAH TRANSISTOR

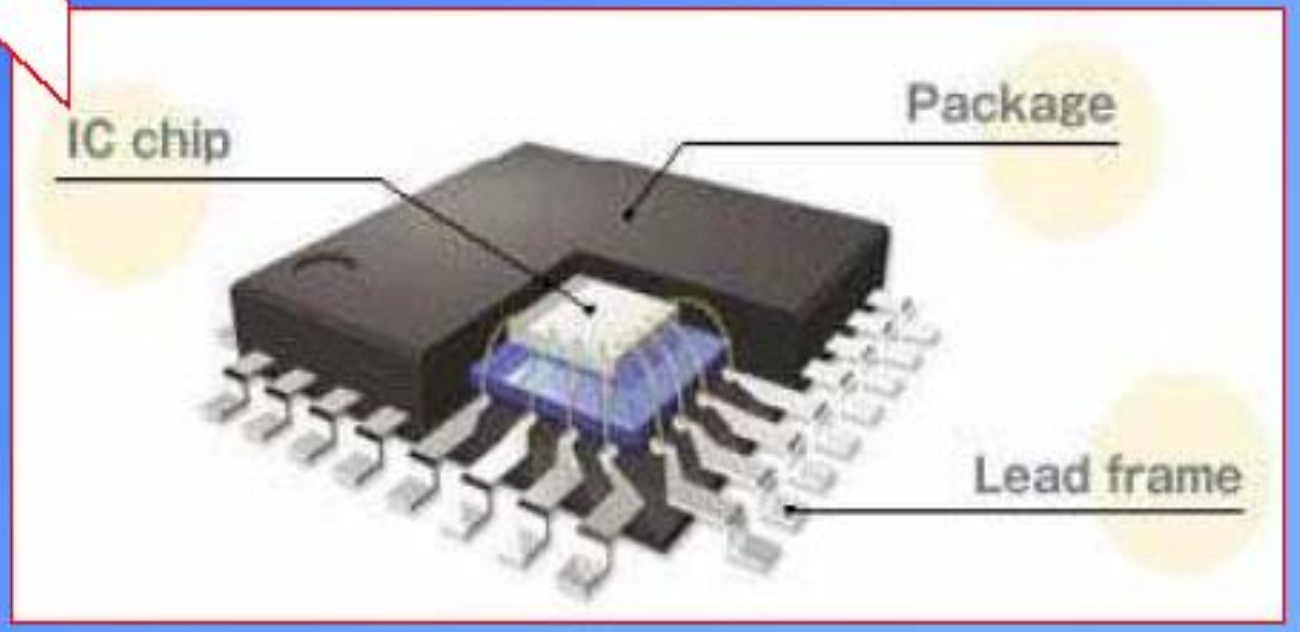
Processor	Transistor count	Date of introduction	Manufacturer	Process	Area
Intel 4004	2,300	1971	Intel	10 µm	12 mm²
Intel 8008	3,500	1972	Intel	10 µm	14 mm²
MOS Technology 6502	3,510[1]	1975	MOS Technology	8 µm	21 mm²
Motorola 6800	4,100	1974	Motorola	6 µm	16 mm²
Quad-core z196[15]	1,400,000,000	2010	IBM	45 nm	512 mm²
Quad-Core + GPU Core i7	1,400,000,000	2012	Intel	22 nm	160 mm²
Dual-Core Itanium 2	1,700,000,000[16]	2006	Intel	90 nm	596 mm²
Six-Core Xeon 7400	1,900,000,000	2008	Intel	45 nm	503 mm²
Quad-Core Itanium Tukwila	2,000,000,000[17]	2010	Intel	65 nm	699 mm²
8-core POWER7+ 80M L3	2,100,000,000	2012	IBM	32 nm	567 mm²
Six-Core Core i7/8-Core Xeon E5 (Sandy Bridge-E/EP)	2,270,000,000 [18]	2011	Intel	32 nm	434 mm²
8-Core Xeon Nehalem-EX	2,300,000,000[19]	2010	Intel	45 nm	684 mm²
10-Core Xeon Westmere-EX	2,600,000,000	2011	Intel	32 nm	512 mm²
Six-core zEC12	2,750,000,000	2012	IBM	32 nm	597 mm²
8-Core Itanium Poulson	3,100,000,000	2012	Intel	32 nm	544 mm²
12-Core POWER8	4,200,000,000	2013	IBM	22 nm	650 mm²
15-Core Xeon Ivy Bridge-EX	4,310,000,000[20]	2014	Intel	22 nm	541 mm²
62-Core Xeon Phi	5,000,000,000	2012	Intel	22 nm	
Xbox One Main SoC	5,000,000,000	2013	Microsoft/AMD	28 nm	363 mm²
SPARC M7	>10,000,000,000	2014	Oracle	20 nm	?

CPU Transistor Counts 1971-2008 & Moore's Law

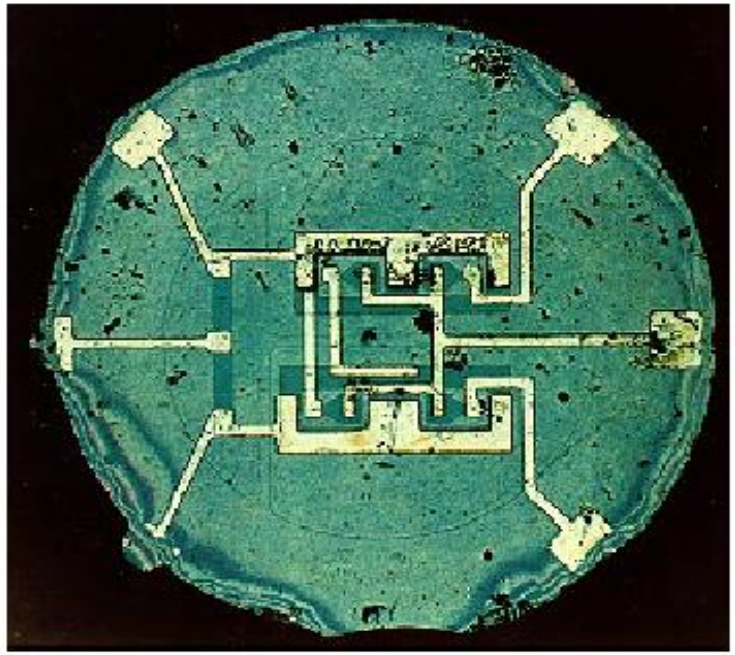


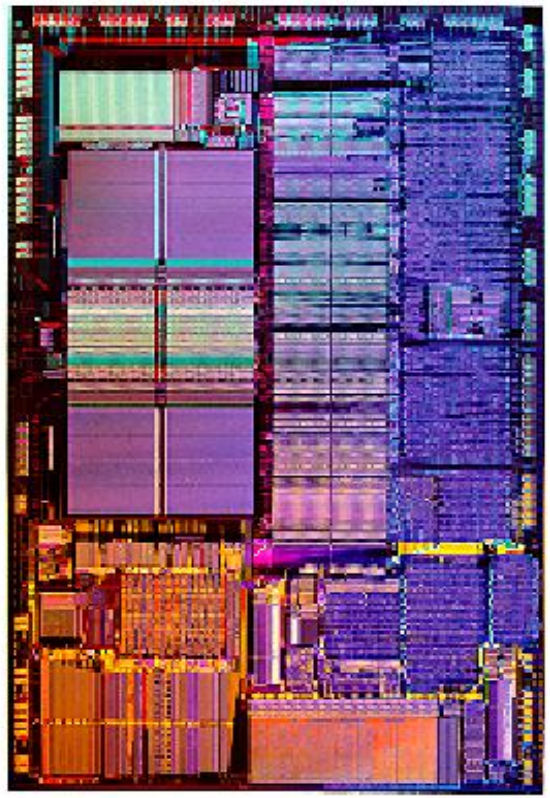
Chip





INTRODUCTION

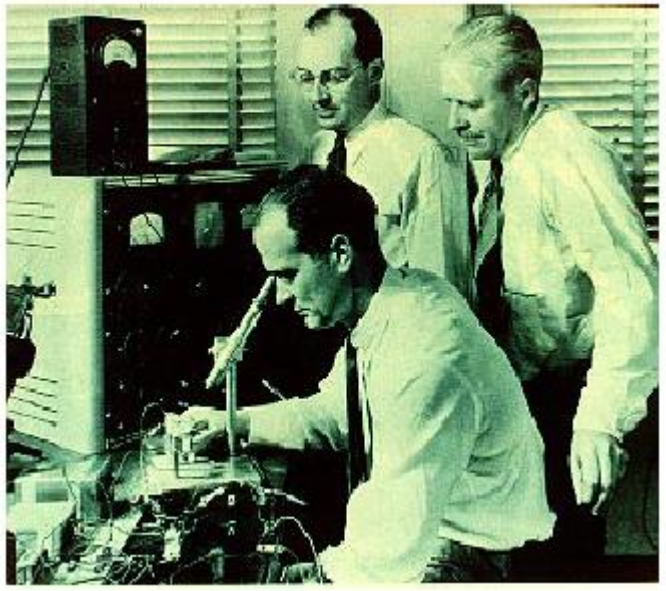


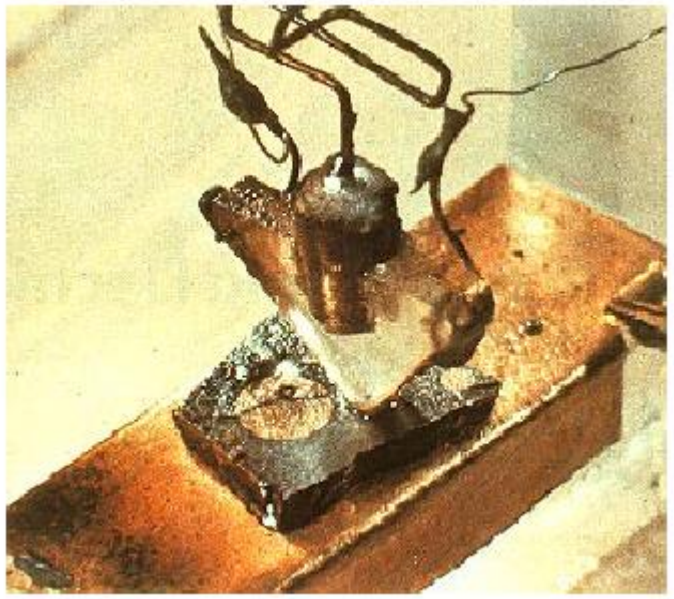


- 1960s and early 1990s integrated circuits.

- Progress due to:
  - Feature size reduction - 0.7X/3 years (Moore's Law).
  - Increasing chip size - ≈ 16% per year.
  - "Creativity" in implementing functions.

THE TRANSISTOR INVENTED AT BELL LAB. IN 1947



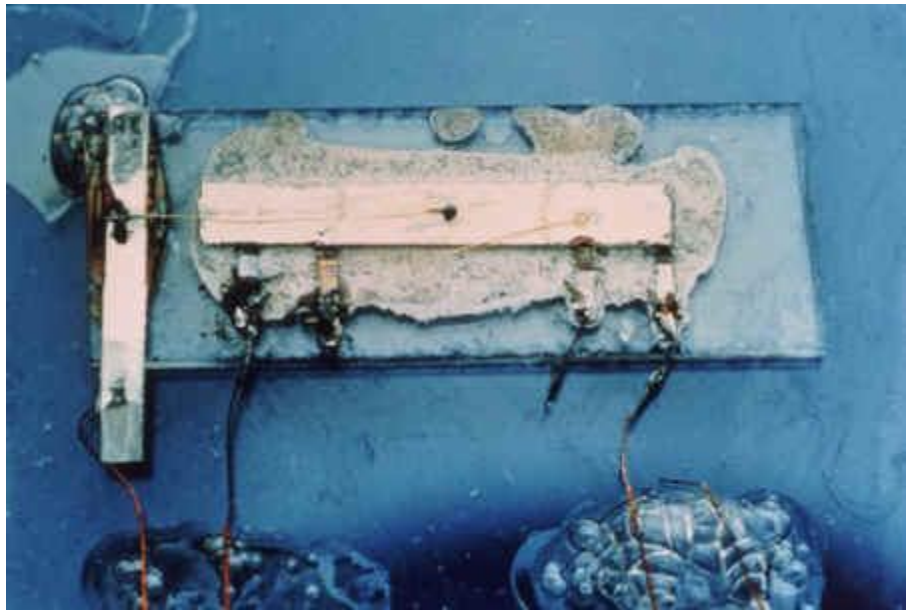


In 1956 the importance of the invention of the transistor by Bardeen, Brattain and Shockley was recognized by the Nobel Prize in physics.

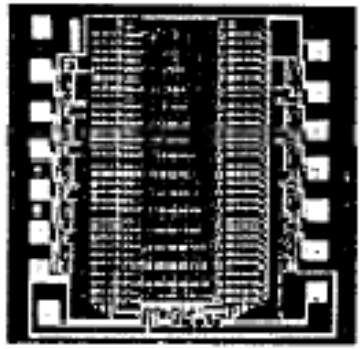
1958 - INTEGRATED CIRCUIT INVENTED

September 12th 1958 Jack Kilby at Texas instrument had built a simple oscillator IC with five integrated components (resistors, capacitors, distributed capacitors and transistors)

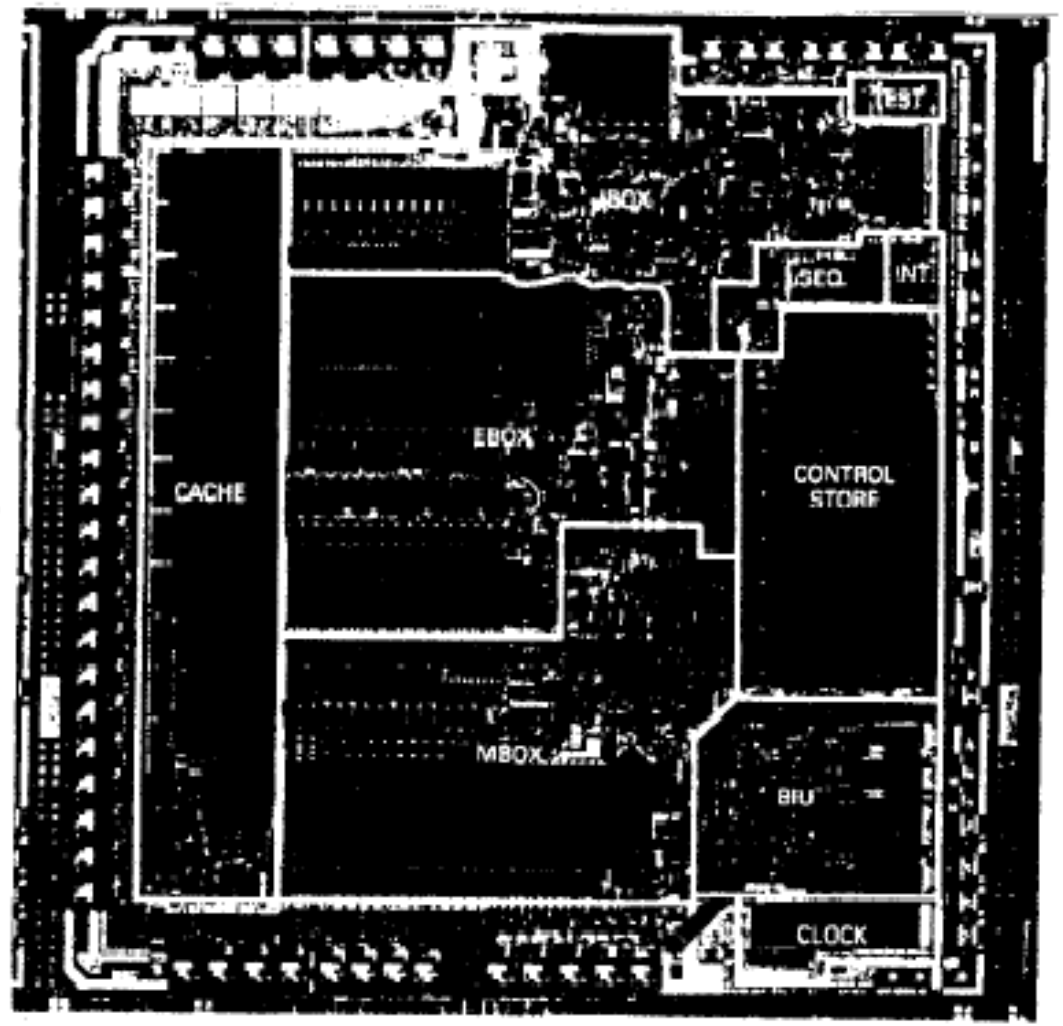
In 2000 the importance of the IC was recognized when Kilby shared the Nobel prize in physics with two others. Kilby was sited by the Nobel committee "*for his part in the invention of the integrated circuit*



a simple oscillator IC



1968



1988

- **ICs manufactured in the 1960s and late 1980s.**

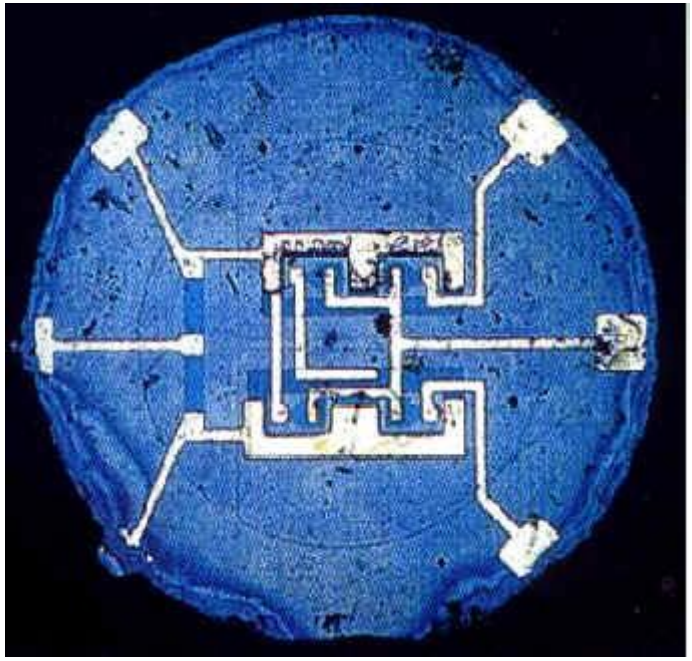
1959 - PLANAR TECHNOLOGY INVENTED

Kilby's invention had a serious drawback, the individual circuit elements were connected together with gold wires making the circuit difficult to scale up to any complexity.

By late 1958 Jean Hoerni at Fairchild had developed a structure with N and P junctions formed in silicon. Over the junctions a thin layer of silicon dioxide was used as an insulator and holes were etched open in the silicon dioxide to connect to the junctions.

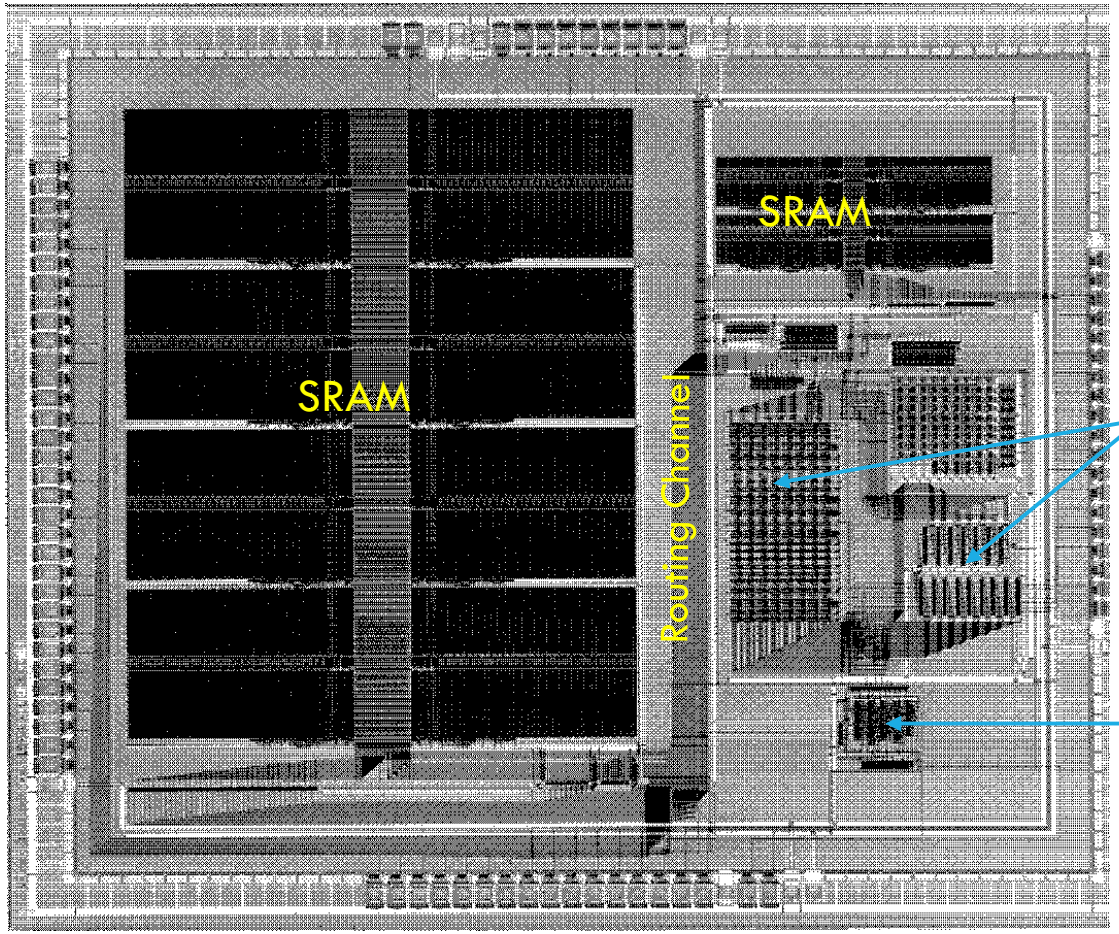
In 1959, Robert Noyce also of Fairchild had the idea to evaporate a thin metal layer over the circuits created by Hoerni's process.

The metal layer connected down to the junctions through the holes in the silicon dioxide and was then etched into a pattern to interconnect the circuit. Planar technology set the stage for complex integrated circuits and is the process used today.



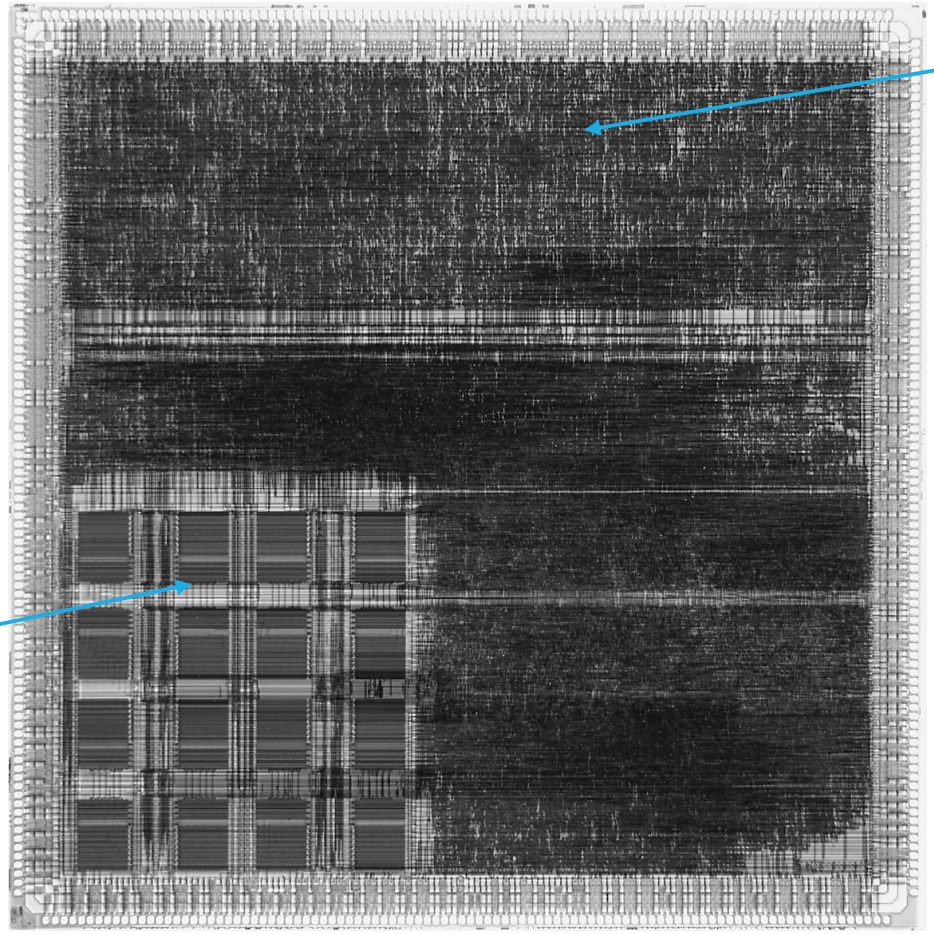
Planar technology

CONTOH DESAIN BERBASIS MACROCELL



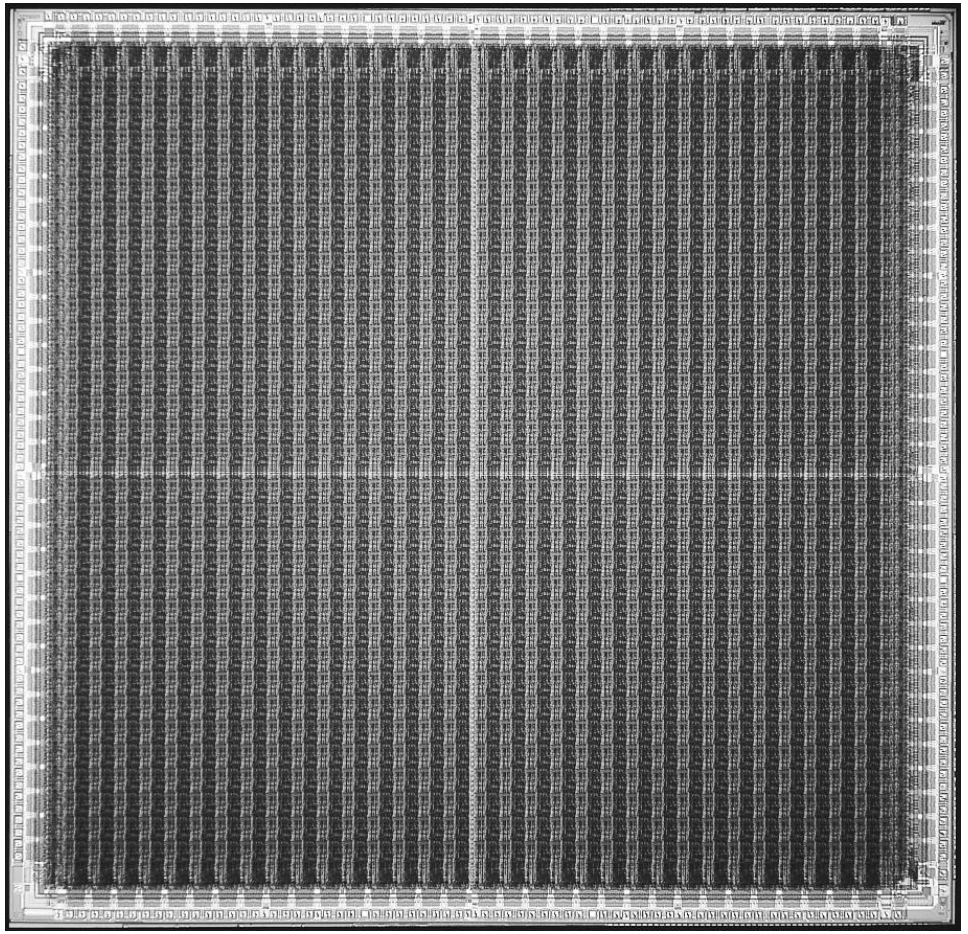
Video-encoder chip
[Brodersen92]

SEA-OF-GATES



LSI Logic LEA300K
(0.6 µm CMOS)

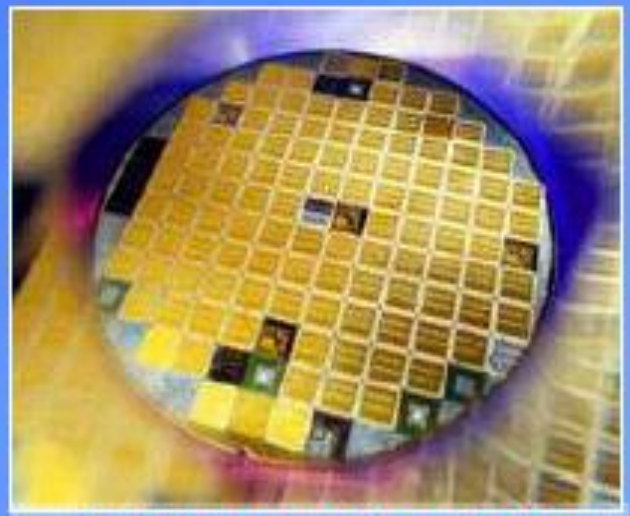
FPGA BERBASIS RAM



Xilinx XC4025

Why VLSI?

- Integration improves the design:
  - lower parasitic = higher speed
  - lower power
  - physically smaller
- Give the control
- High Performance
- Easier to design
- Integration reduces manufacturing cost-(almost) no manual assembly.

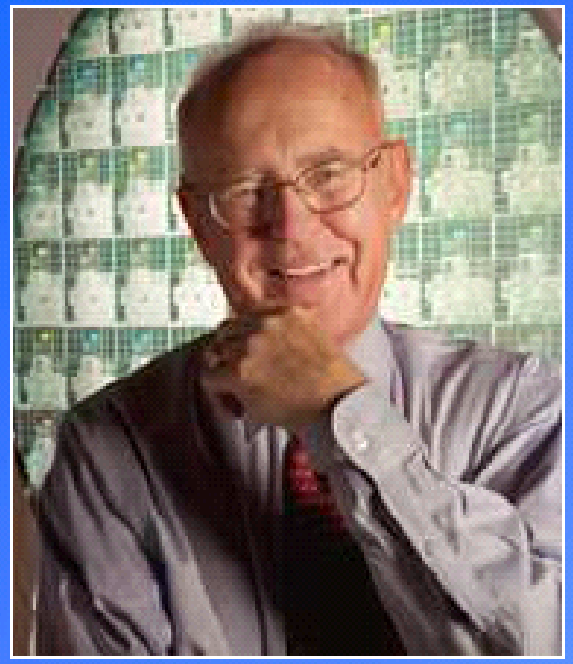


300 mm wafers & 90 nano-Technology

Integration Levels

SSI:	10 gates
MSI:	1000 gates
LSI:	10,000 gates
VLSI:	> 10k gates

Gordon Moore's Law (1969)

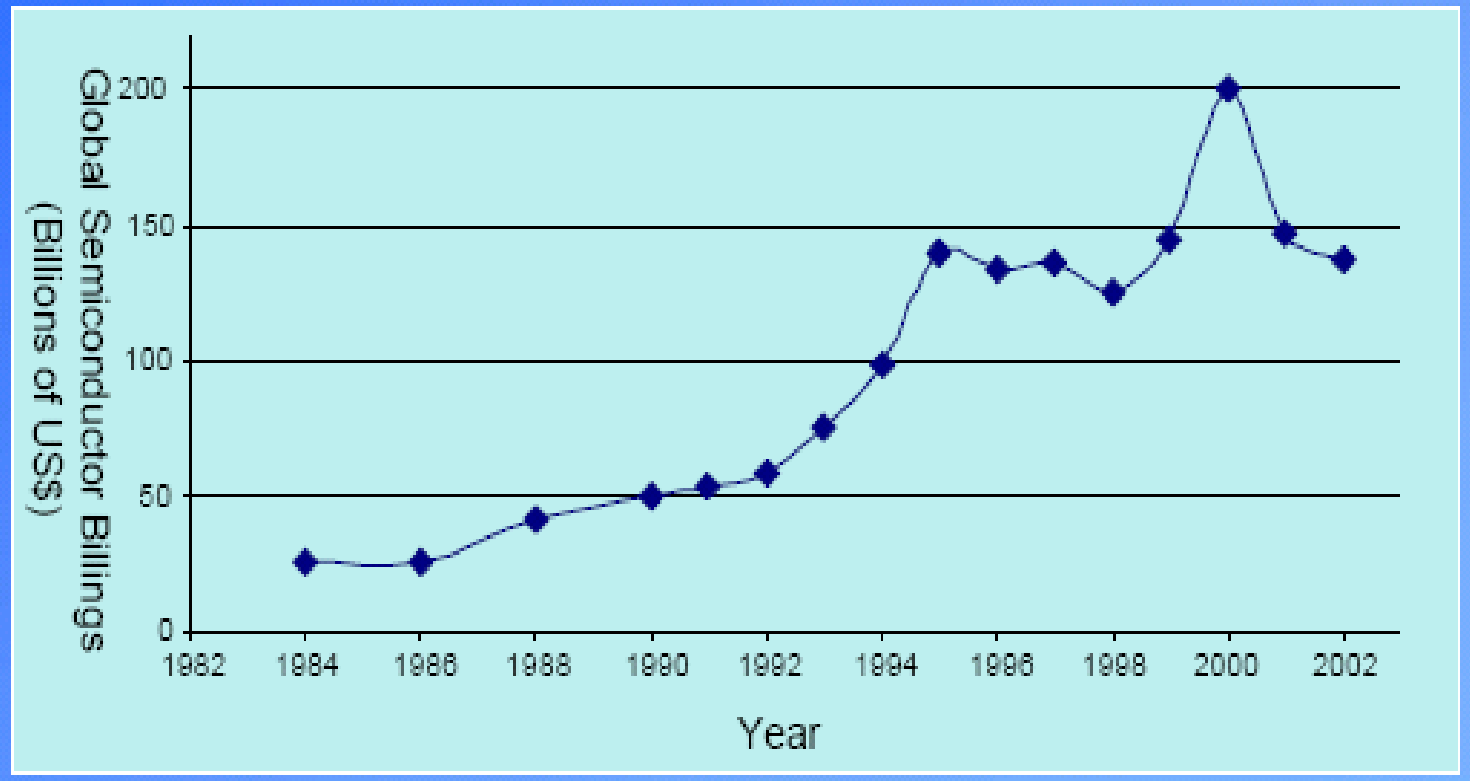


co-founder of Intel.

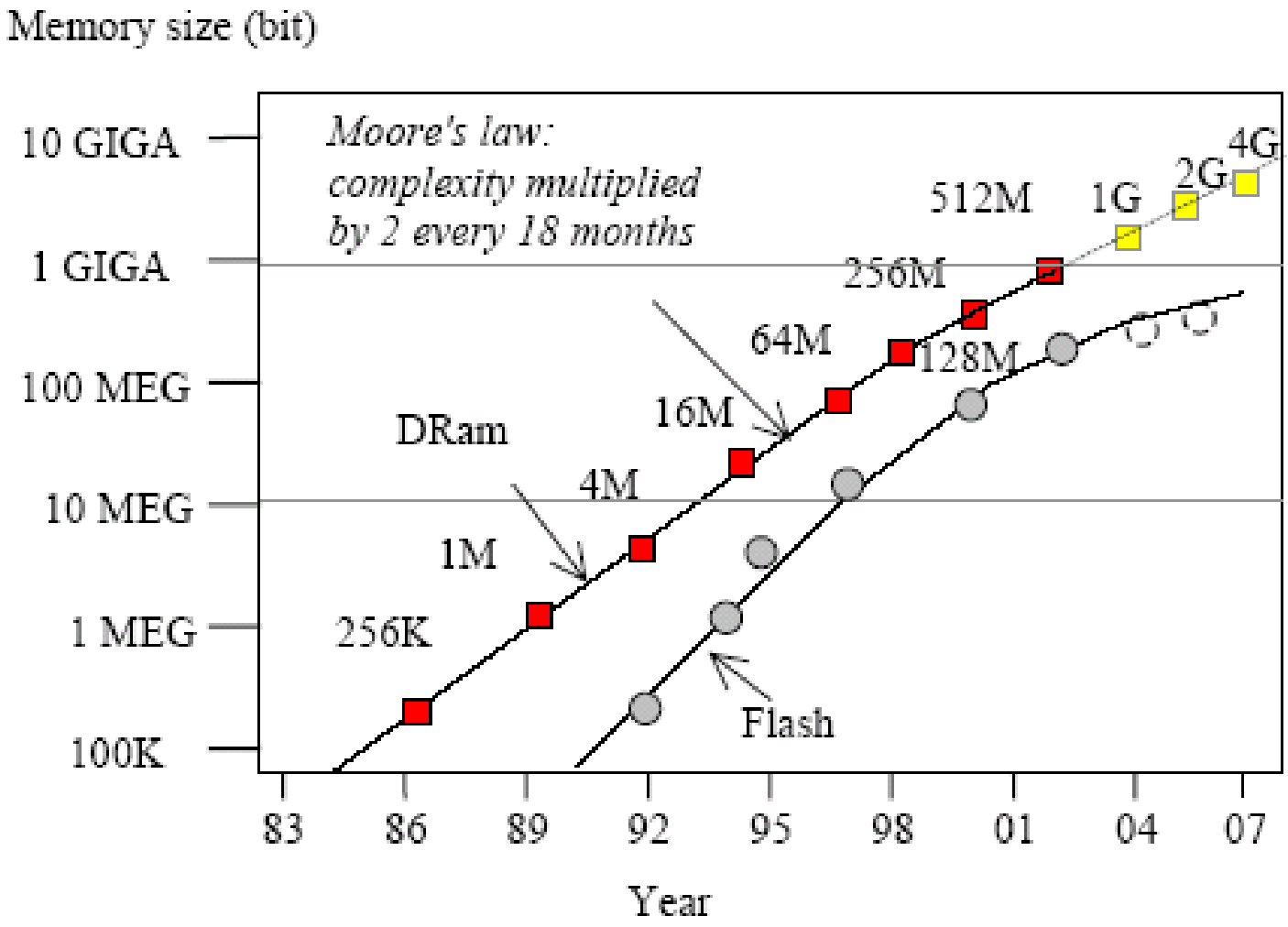
- Two components:
  - Transistor dimensions reduce by 10.5% every year
    - Density increases 22.1% every year
  - Additional 22% increase every year due to:
    - Wafer and chip size increases
    - Circuit design and fabrication process innovations
- 44% transistor count increase in microprocessors every year
  - Transistor count more than doubles every 2 years

Annual Sales

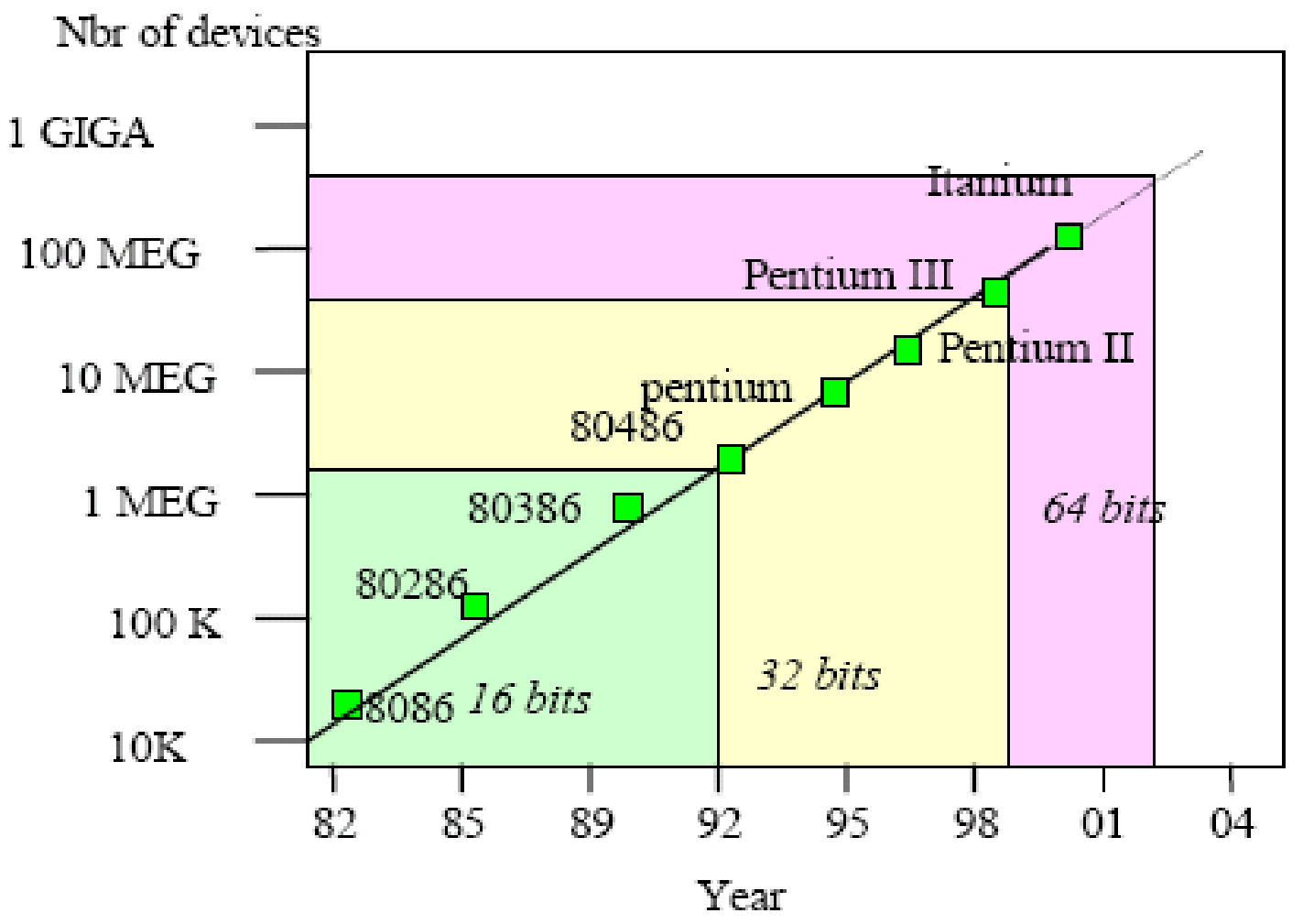
- 10^{18} transistors manufactured in 2003
  - 100 million for every human on the planet



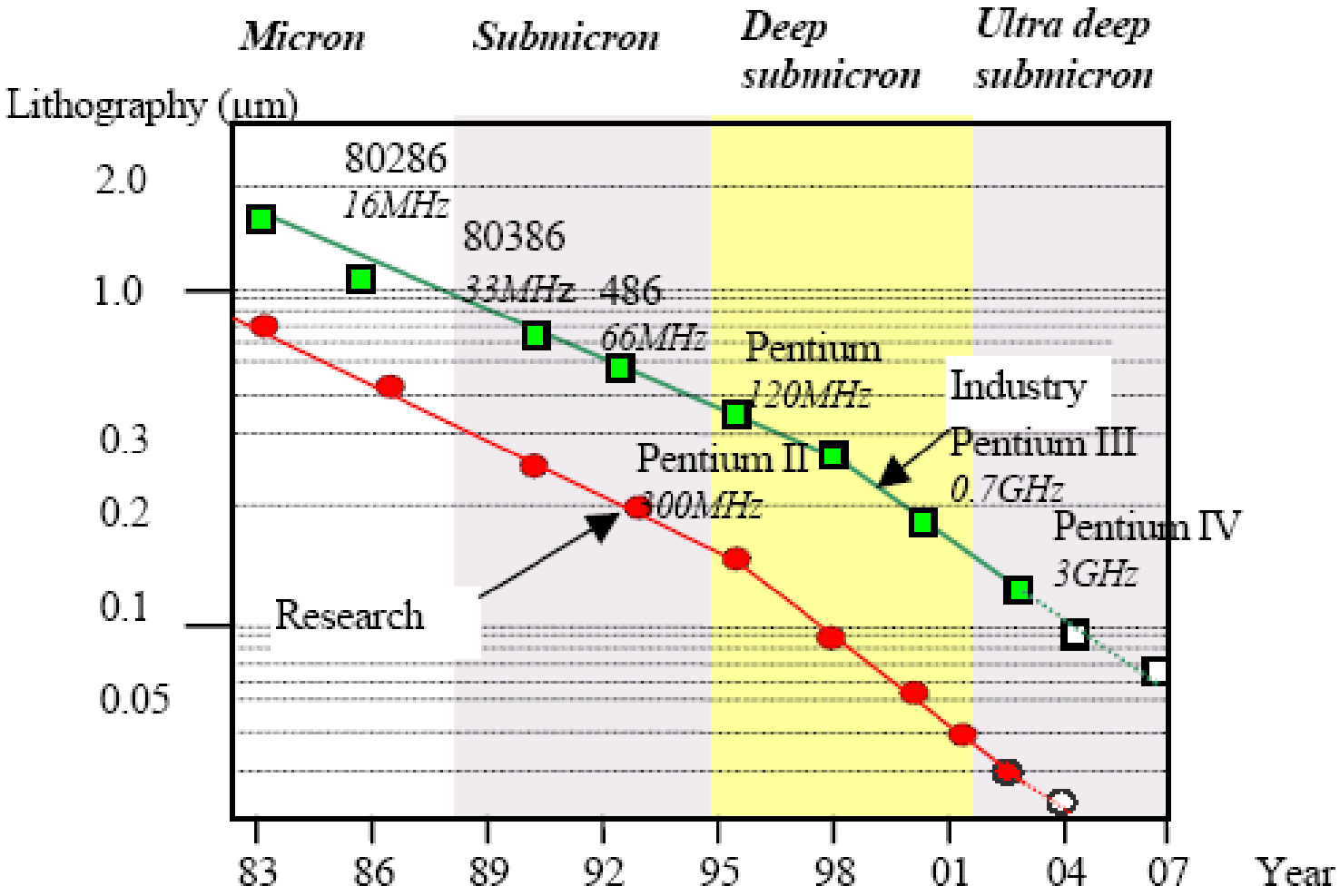
EVOLUTION OF MEMORY



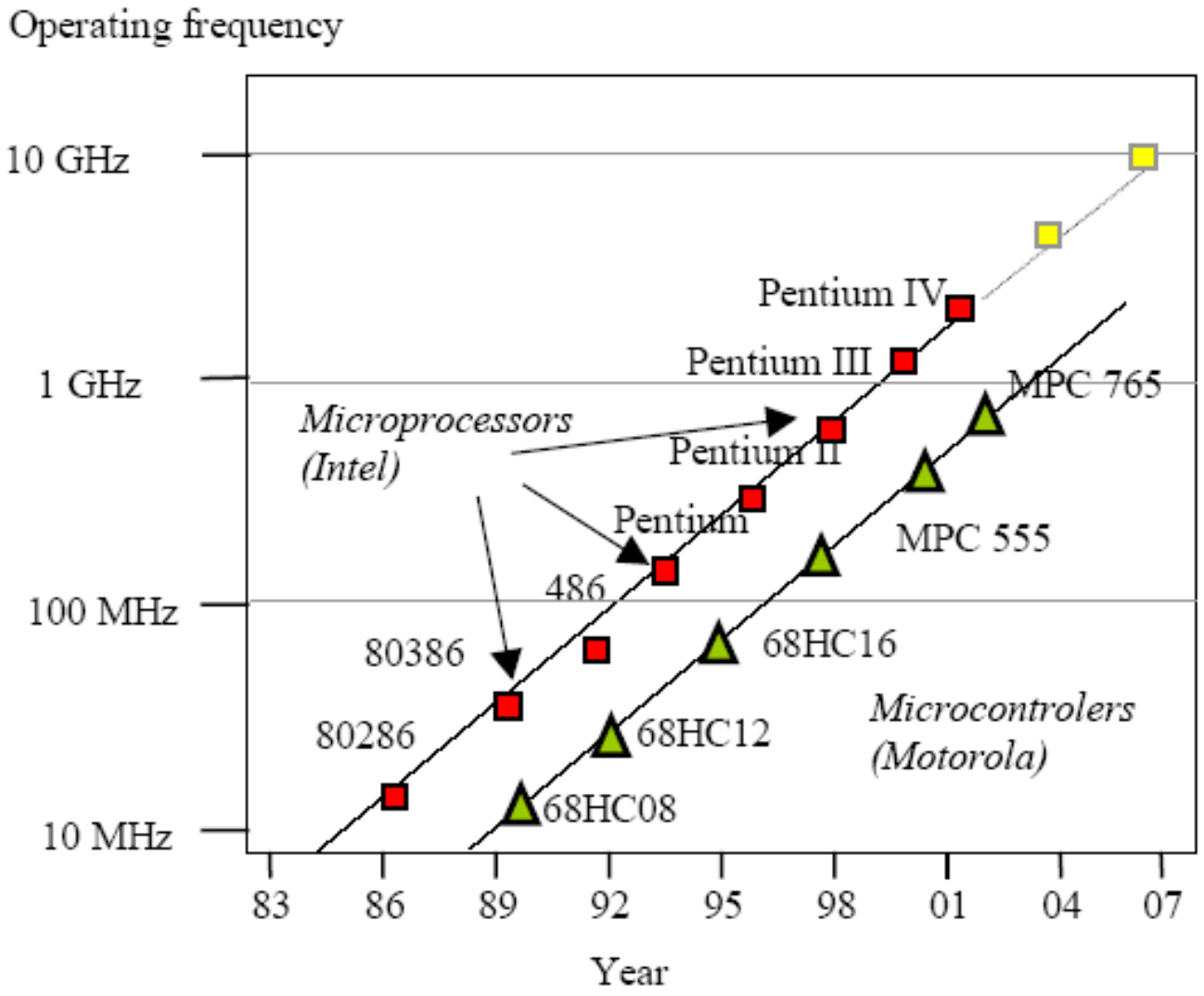
EVOLUTION OF MICROPROCESSOR



EVOLUTION OF LITHOGRAPHY



FREQUENCY IMPROVEMENTS



Summary of INTEL Processor

- 10^4 increase in transistor count, clock frequency over 30 years!

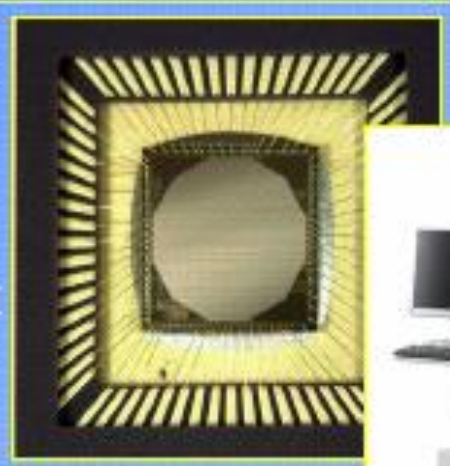
Table 4.19 History of Intel microprocessors over three decades

Processor	Year	Feature Size (μm)	Transistors	Frequency (MHz)	Word size	Package
4004	1971	10	2.3k	0.75	4	16-pin DIP
8008	1972	10	3.5k	0.5–0.8	8	18-pin DIP
8080	1974	6	6k	2	8	40-pin DIP
8086	1978	3	29k	5–10	16	40-pin DIP
80286	1982	1.5	134k	6–12	16	68-pin PGA
Intel386	1985	1.5–1.0	275k	16–25	32	100-pin PGA
Intel486	1989	1–0.6	1.2M	25–100	32	168-pin PGA
Pentium	1993	0.8–0.35	3.2–4.5M	60–300	32	296-pin PGA
Pentium Pro	1995	0.6–0.35	5.5M	166–200	32	387-pin MCM PGA
Pentium II	1997	0.35–0.25	7.5M	233–450	32	242-pin SECC
Pentium III	1999	0.25–0.18	9.5–28M	450–1000	32	330-pin SECC2
Pentium 4	2001	0.18–0.13	42–55M	1400–3200	32	478-pin PGA

The Cost of Fabrication

- Current cost: $2-3 billion
- Most profitable period is first 18 months-2 years

- Cost factors in ICs
  - For large-volume ICs:
    - Packaging is largest cost
    - Testing is second-largest cost
  - For low-volume ICs:
    - Design costs may swamp all manufacturing costs



Cost of Integrated Circuits

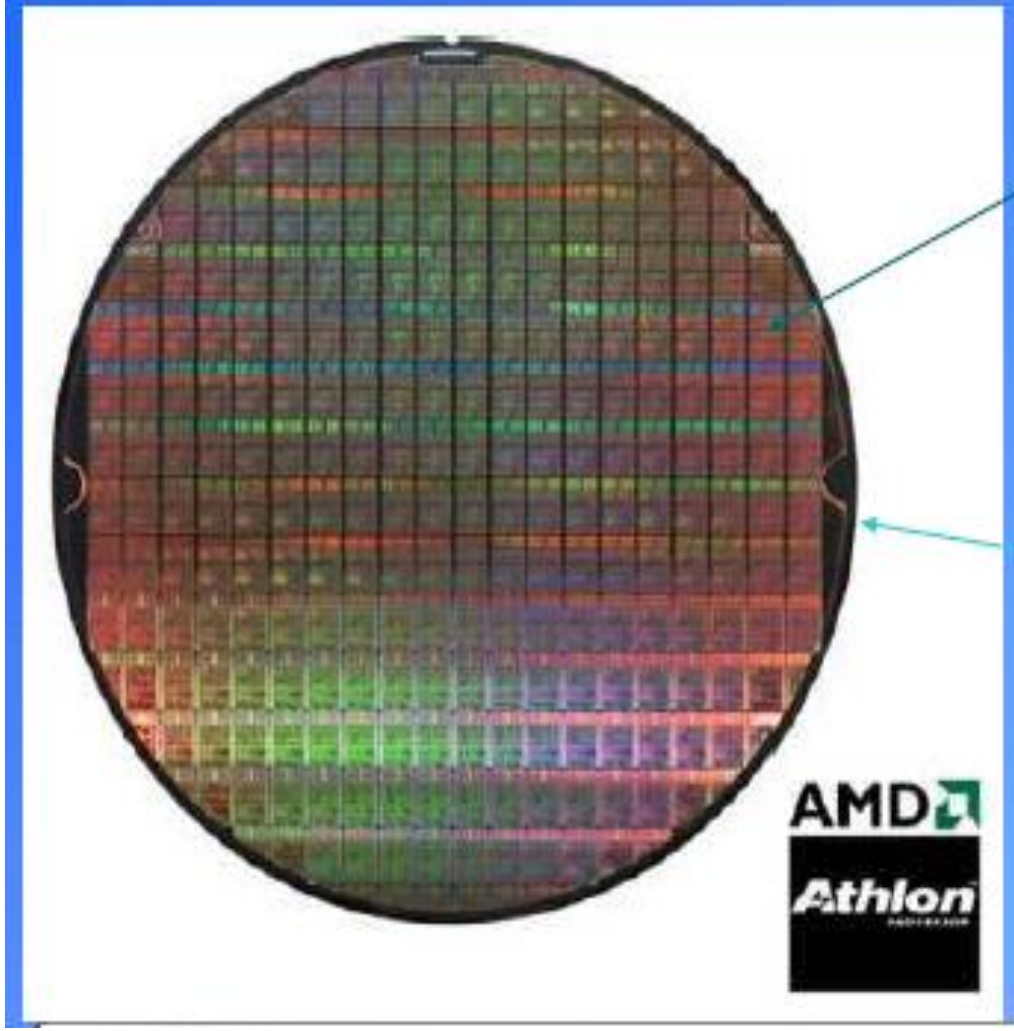
$$\text{cost per IC} = \text{variable cost per IC} + \left(\frac{\text{fixed cost}}{\text{volume}}\right)$$

$$\text{variable cost per IC} = \frac{\text{cost of die} + \text{cost of test} + \text{cost of package}}{\text{yield}}$$

$$\text{yield} = \frac{\text{number ICs satisfy ALL requirements}}{\text{total number of ICs fabricated}}$$

- FIXED COST:
  - engineering cost, research and development, indirect costs.
- VARIABLE COST:
  - die cost, test cost, package cost

Die Cost

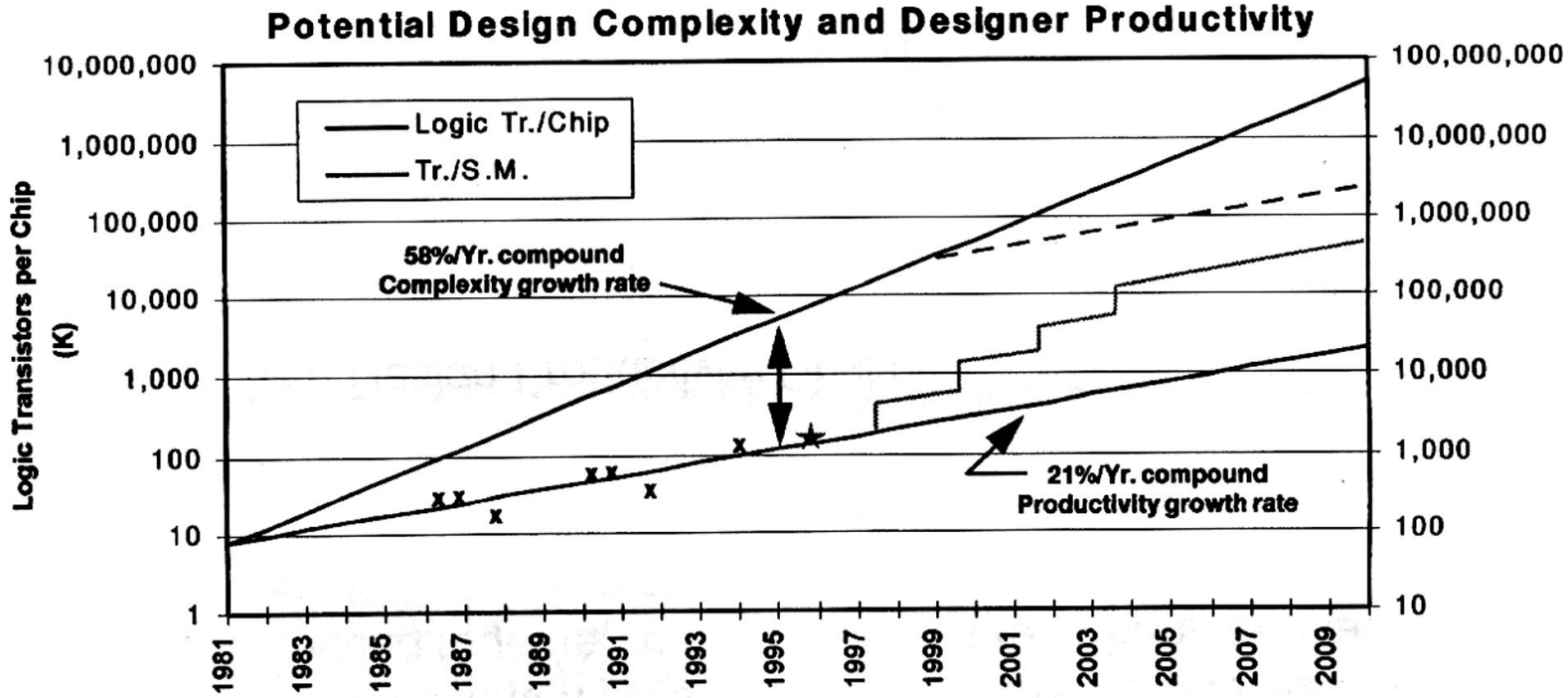


Single die

Wafer

Going up to 12″ (30cm)

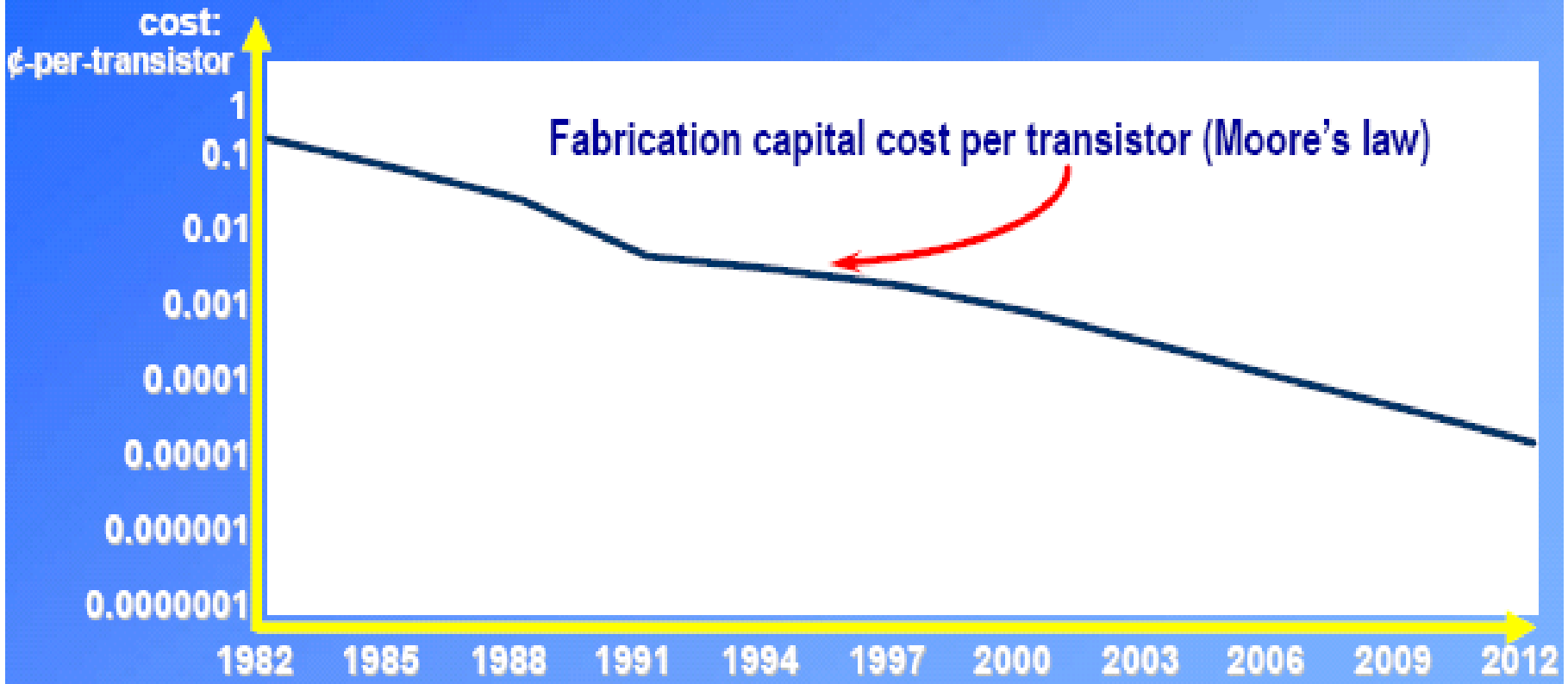
THE DESIGN PROBLEM



A growing gap between design complexity and design productivity

Source: sematech97

Cost per Transistor



Birth of Modern Electronics -- 1947

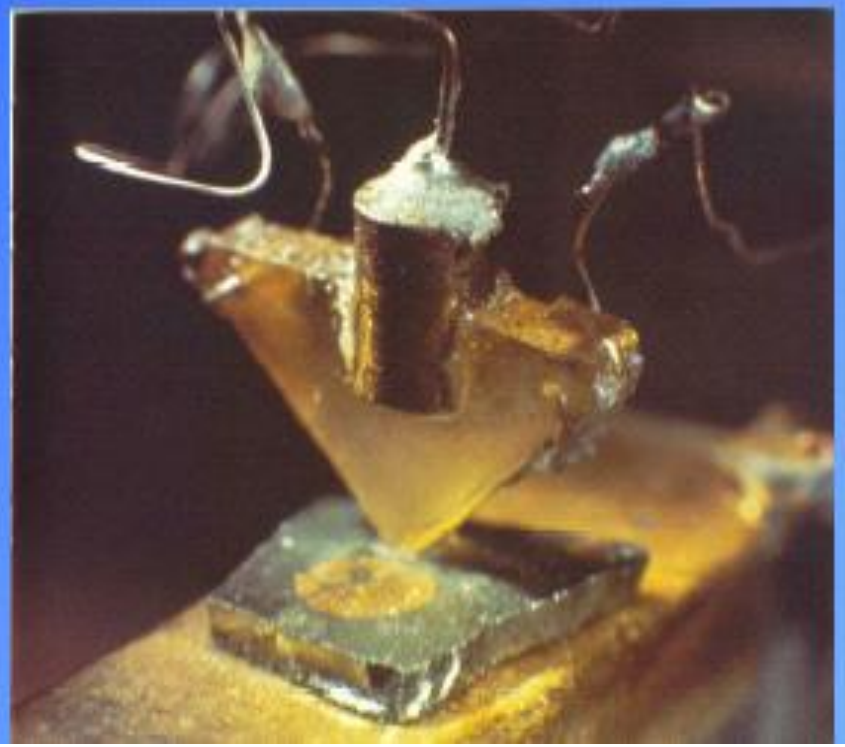
AT&T Bell Laboratories -- Invention of Point Contact Transistor

William Shockley, Walter Brittain, and John Bardeen

Winners of the 1956 Nobel Prize in Physics

Vacuum tubes ruled in first half of 20th century

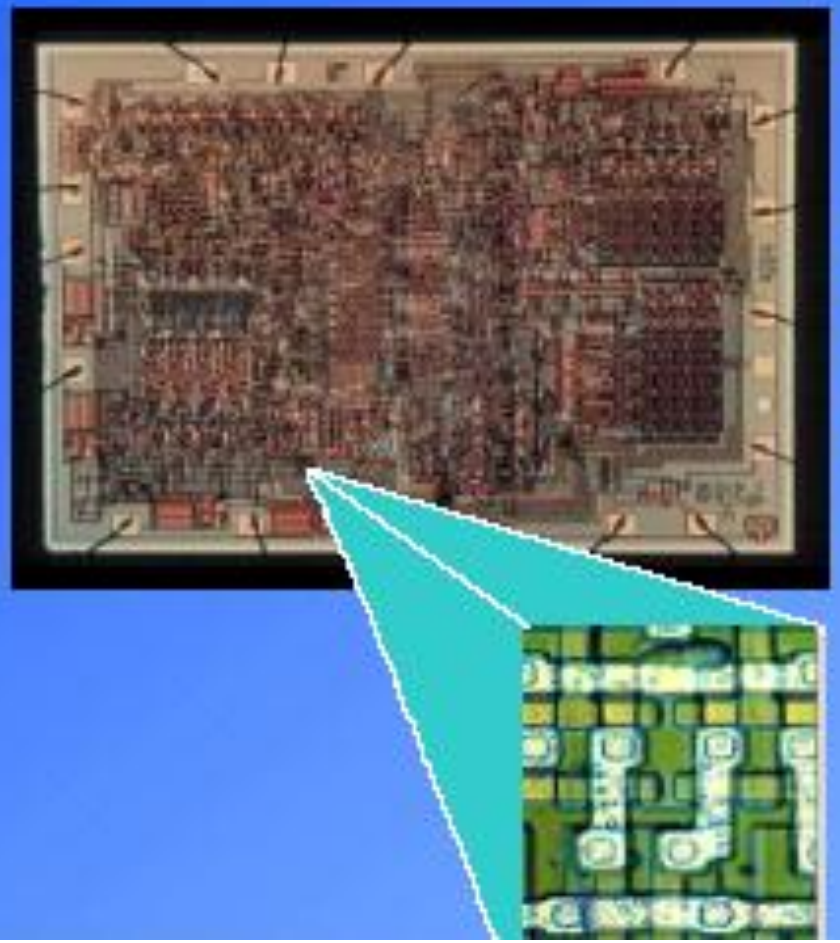
Large, expensive, power-hungry, unreliable



***Read* Crystal Fire**

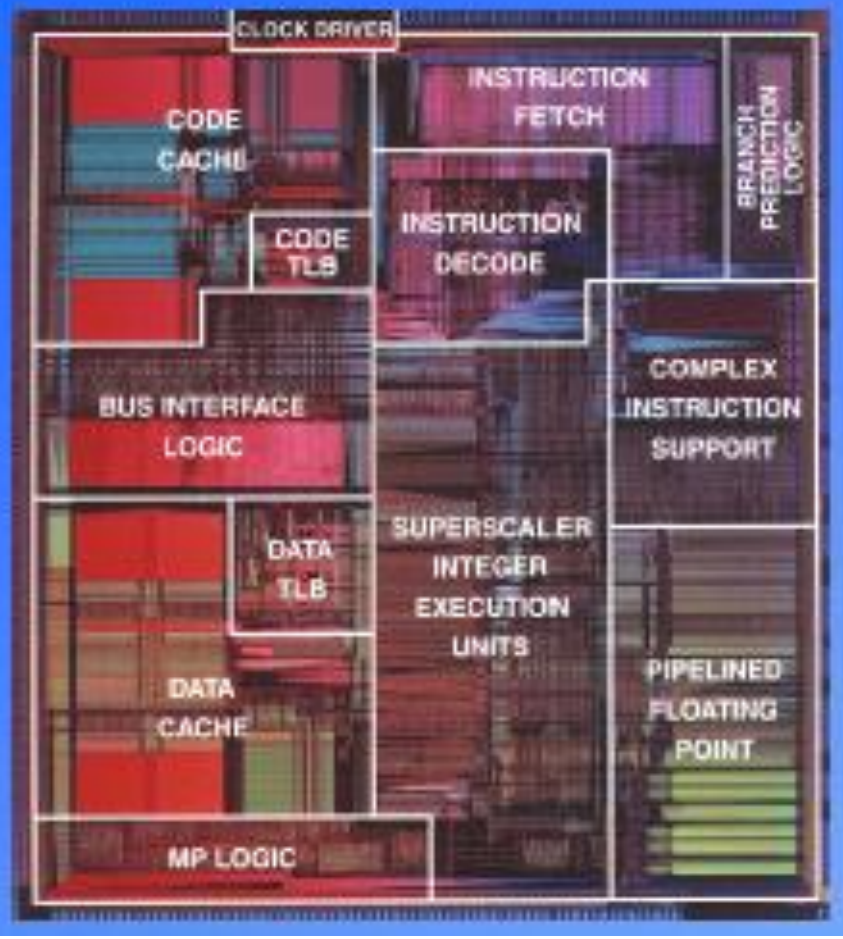
by Riordan, Hoddeson

Intel 4004 Die Photo



- Introduced in 1970
  - First microprocessor
- 2,250 transistors
- 12 mm^2
- 108 KHz

Pentium Die Photo



- 3,100,000 transistors
- 296 mm^2
- 60 MHz
- Introduced in 1993
  - 1st superscalar implementation of IA32

VLSI TECHNOLOGY?

Integration improves the design

- Lower parasitics = higher speed
- Lower power consumption
- Physically smaller

Integration reduces manufacturing cost - (almost) no manual assembly

VLSI APPLICATIONS

VLSI is an implementation technology for electronic circuitry - analogue or digital

It is concerned with forming a pattern of interconnected switches and gates on the surface of a crystal of semiconductor

Microprocessors

- personal computers
- microcontrollers

Memory - DRAM / SRAM

Special Purpose Processors - ASICS (CD players, DSP applications)

Optical Switches

Has made highly sophisticated control systems mass-producable and therefore cheap

MOORE'S LAW

Gordon Moore: co-founder of Intel

Predicted that the number of transistors per chip would grow exponentially (double every 18 months)

Exponential improvement in technology is a natural trend:

- e.g. Steam Engines - Dynamo - Automobile

THE COST OF FABRICATION

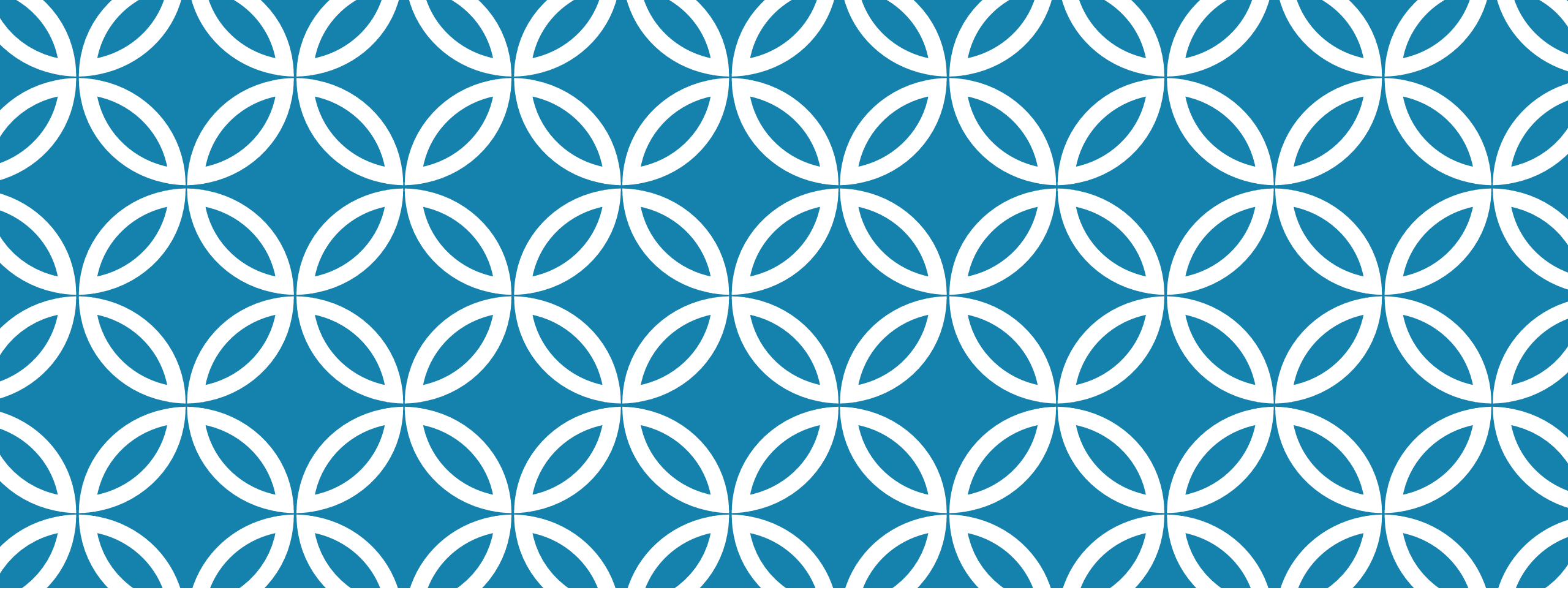
Current cost $2 - 3 billion

Typical fab line occupies 1 city block, employees a few hundred employees

Most profitable period is first 18 months to 2 years

For large volume IC's packaging and testing is largest cost

For low volume IC's, design costs may swamp manufacturing costs



TECHNOLOGY BACKGROUND

WHAT IS A SILICON CHIP?

A pattern of interconnected switches and gates on the surface of a crystal of semiconductor (typically Si)

These switches and gates are made of

- areas of n-type silicon
- areas of p-type silicon
- areas of insulator
- lines of conductor (interconnects) joining areas together
  - Aluminium, Copper, Titanium, Molybdenum, polysilicon, tungsten

The geometryof these areas is known as the layout of the chip

Connections from the chip to the outside world are made around the edge of the chip to facilitate connections to other devices

SWITCHES

Digital equipment is largely composed of switches

Switches can be built from many technologies

- relays (from which the earliest computers were built)
- thermionic valves
- transistors

The perfect digital switch would have the following:

- switch instantly
- use no power
- have an infinite resistance when off and zero resistance when on

Real switches are not like this!

SEMICONDUCTORS AND DOPING

Adding trace amounts of certain materials to semiconductors alters the crystal structure and can change their electrical properties

- in particular it can change the number of free electrons or holes

N-Type

- semiconductor has free electrons
- dopant is (typically) phosphorus, arsenic, antimony

P-Type

- semiconductor has free holes
- dopant is (typically) boron, indium, gallium

Dopants are usually implanted into the semiconductor using Implant Technology, followed by thermal process to diffuse the dopants

IC TECHNOLOGY

Speed / Power performance of available technologies

The microelectronics evolution

SIA Roadmap

Semiconductor Manufacturers 2001 Ranking

METAL-OXIDE-SEMICONDUCTOR (MOS) AND RELATED VLSI TECHNOLOGY

- pMOS
- nMOS
- CMOS
- BiCMOS
- GaAs

BASIC MOS TRANSISTORS

Minimum line width

Transistor cross section

Charge inversion channel

Source connected to substrate

Enhancement vs Depletion mode devices

pMOS are 2.5 time slower than nMOS due to electron and hole mobilities

FABRICATION TECHNOLOGY

Silicon of extremely high purity

- chemically purified then grown into large crystals

Wafers

- crystals are sliced into wafers
- wafer diameter is currently 150mm, 200mm, 300mm
- wafer thickness <1mm
- surface is polished to optical smoothness

Wafer is then ready for processing

Each wafer will yield many chips

- chip die size varies from about 5mmx5mm to 15mmx15mm
- A whole wafer is processed at a time

FABRICATION TECHNOLOGY

Different parts of each die will be made P-type or N-type (small amount of other atoms intentionally introduced - doping -implant)

Interconnections are made with metal

Insulation used is typically SiO2. SiN is also used. New materials being investigated (low-k dielectrics)

FABRICATION TECHNOLOGY

nMOS Fabrication

CMOS Fabrication

- p-well process
- n-well process
- twin-tub process

FABRICATION TECHNOLOGY

All the devices on the wafer are made at the same time

After the circuitry has been placed on the chip

- the chip is overglassed (with a passivation layer) to protect it
- only those areas which connect to the outside world will be left uncovered (the pads)

The wafer finally passes to a test station

- test probes send test signal patterns to the chip and monitor the output of the chip

The *yield* of a process is the percentage of die which pass this testing

The wafer is then scribed and separated up into the individual chips. These are then packaged

Chips are 'binned' according to their performance

CMOS TECHNOLOGY

First proposed in the 1960s. Was not seriously considered until the severe limitations in power density and dissipation occurred in NMOS circuits

Now the dominant technology in IC manufacturing

Employs both pMOS and nMOS transistors to form logic elements

The advantage of CMOS is that its logic elements draw significant current only during the transition from one state to another and very little current between transitions - hence power is conserved.

In the case of an inverter, in either logic state one of the transistors is off. Since the transistors are in series, (~ no) current flows.

See twin-well cross sections

BICMOS

A known deficiency of MOS technology is its limited load driving capabilities (due to limited current sourcing and sinking abilities of pMOS and nMOS transistors.

Bipolar transistors have

- higher gain
- better noise characteristics
- better high frequency characteristics

BiCMOS gates can be an efficient way of speeding up VLSI circuits

See table for comparison between CMOS and BiCMOS

CMOS fabrication process can be extended for BiCMOS

Example Applications

- CMOS - Logic
- BiCMOS- I/O and driver circuits
- ECL - critical high speed parts of the system