DESIGN OF 16 TO 1 MULTIPLEXER IC USING HIGH SPEED CMOS TECHNOLOGY

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ABSTRACT: In this research is designed a digital multiplexer IC of 16 to 1 High Speed Complementary Metal Oxide Semiconductor (HCMOS) for digital circuit applications. The purpose of this research is an analysis to improve the CMOS characteristic such as Voltage Transfer Characteristic (VTC), propagation delay, and power dissipation, *ie*: to minimize the value of propagation delay and power dissipation than previous CMOS design. The HCMOS schematic and layout was drawn in DSCH and Microwind2 software, respectively. A PSpice simulation software was used to test the schematic characteristic. A 5 volt DC power supply was used in this schematic design and coupling capacitor was ≤ 5pF. We used the maximum frequence, K_N, K_P parameters of 10 MHz, 40 µA/V^2 and 16µA/V^2, respectively. This design is supposed to be an average propagation delay of less than 70 ns.

The result of research shows that VTC are V_{IL} = 2.92 volt, V_{OL} = 0 volt, V_{IH} = 2.94 volt, and V_{OH} = 5 volt; then the Noise Margins are N_{MH} = 2.06V and N_{ML} = 2.92V. The simulation result of time propagation delay are t_{PLH} = 9.79 ns, t_{PHL} = 3.92 ns, and t_{PD} = 6.85 ns. The output of power dissipation is 125µW. The design of schematic layout area without I/O pad is 1189,1 µm x 23,3 µm and the area with I/O pad is 1625.5 µm x 1625.5 µm. Based on simulation results show that the specification and design of 16 to 1 Multiplexer IC by using High Speed CMOS technology (HCMOS) has the speed 13.43 ns faster than DM74150 TTL and 152.25 ns faster than MM54C150J CMOS IC. Comparing to the both of ICs, the power dissipation of this design is 109.91 nJ lower than CMOS and 6.792 nJ lower than TTL IC.

1. INTRODUCTION

Integrated Circuits (ICs) have been developed by industries for electronic applications, especially in the fields of computer, control, and sensors (Lantz, 2009). Bipolar IC technology typically has a small time propagation delay, so it can work in high speed. On the other hand, bipolar technology like TTL has a disadvantage for the high power dissipation. Now, CMOS replaces the bipolar technology that has the advantages of low power dissipation, high fan out, and the noise margin is better than bipolar (Piguet, 2006). But CMOS Propagation delay is slower when moving loads with large capacitance. High Speed CMOS (HCMOS) is the CMOS technology that designed specially so that it has a propagation delay equal to or better than bipolar technology (Sicard, 2007) mainly to drive the load with large capacitance. In this research, HCMOS is design for 16 to 1 digital Multiplexer with ideal condition and maximize its performance.

2. METHOD

The method in this research is based on steps to design the 16 to 1 HCMOS IC include design of the logic gate schematic, CMOS specification, transistor parameters, and W/L ratio, Voltage Transfer Characteristic, propagation delay, and layout drawing. The HCMOS schematic was drawn in DSCH software and the layout was drawn by Microwind2 software. The steps were done not only schematic design the layout, but also the analysis and simulation to optimized the speed and improve the IC performances. The PSpice software was used for simulation.

2.1 Schematic Design

The schematic design configuration of multiplexer is shown in Figure 1(a). The truth table based on the logic function of Multiplexer is shown in Table 1. The Output of Multiplexer is controlled by combination of the four selector pins (S0-S3) that has 2^4 selection possibilities from 16 input pins. Based on gate configuration, the fundamental difference between CMOS and HCMOS Multiplexer configuration is the presence of the inverter pair

series in HCMOS. This circuit configuration takes the advantage of inverter pair that called cascade driver. This Multiplexer consist of five inverter gates are composed from 10 PMOS and NMOS transistors, five inputs of 16 NAND gates are composed 160 PMOS and NMOS transistors, 16 inputs of NAND gates are composed from 32 PMOS and NMOS transistor, and a cascade inverter is composed from four PMOS and NMOS transistors. So the number of CMOS transistors are 206 transistors. Figure 1(b) shows the CMOS transistor schematic configuration of 16 to 1 Multiplexer.

Table 1. Truth Table of 16 to1 HCMOS Multiplexer

Select input				output
S0	S1	S2	S3	Y
L	L	L	L	I0
L	L	L	H	I1
L	L	H	L	I2
L	L	H	H	I3
L	H	L	L	I4
L	H	L	H	I5
L	H	H	L	I6
L	H	H	H	I7
H	L	L	L	I8
H	L	L	H	I9
H	L	H	L	I10
H	L	H	H	I11
H	H	L	L	I12
H	H	L	H	I13
H	H	H	L	I14
H	H	H	H	I15

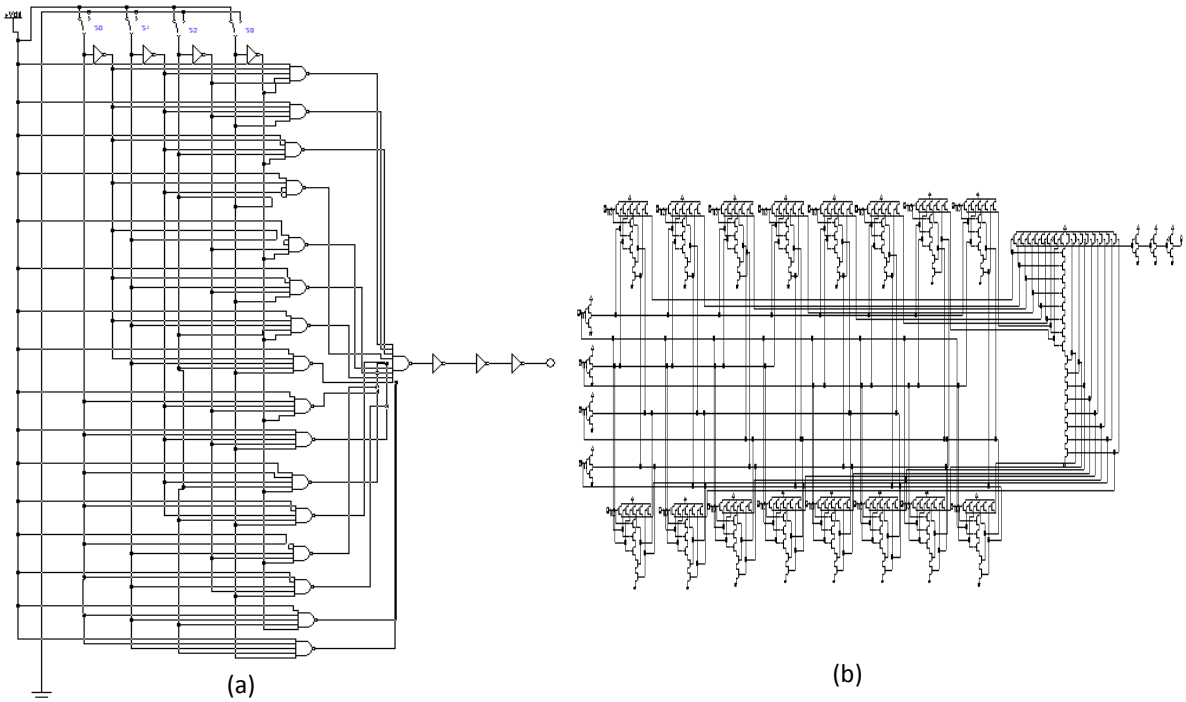

Figure 1. Logic Gate Circuit (a) and Transistor Schematic (b) of 16 to 1 Multiplexer

2.2 Design Parameters

A schematic characteristic of Multiplexer design was determined based on the characteristic of basic logic gate which depend on device material of transistor. A kind of basic parameters are ε_{0x}= 3.45x10^{-13} F/cm, μ_e/μ_n=580 cm^2/V.s (NMOS), μ_n/μ_p=230 cm^2/V.s (PMOS), V_T=0.8 (NMOS), V_T= -0.8 (PMOS), V_{DD}=5V, K_N=300 μA/V^2, K_P=120 μA/V^2, t_{ox}=15nm, $2\phi_f$ =0.3V, and γ=0.4V which is suitable from owner manual and rule of supporting software from Microwind2. It has configuration of 0.6 µm CMOS. The *W* and *L* value for n-type and p-type MOS at basic gate determined by consideration of interaction between input and output voltage. Determination of W and L of CMOS inverter based on analysis from K_R=1 to obtain the voltage transfer characteristic of symmetrical input and output. The parameter can be determined by μ_n=580 cm²/V.s and μ_p =230 cm²/V.s, then ratio of Kn/Kp is 2.5. A cross analysis and IC design rule were done to determine W/L value each transistor. A wide of polysilicon in the cross section of MOS transistor is notated by L and wide of diffusion notated by W. According to the minimum size of polysilicon is 2λ, the value of W_p and W_n are 4λ and 10λ. Inside of Microwind2 software (,6µm CMOS Process),

the λ is 0.3µm. It can be determined that in the first cascade of the W_p =W_n and L_p=L_n are 3.6 and 0.6 µm, respectively. The value of W_p=W_n in second cascade are 10.8 and 0.6 µm for L_p=L_n.

2.3 Noise Margin

The noise margin of logic gate calculated from V_{IH}, V_{IL}, V_{OH}, and V_{OL} by transistor parameters. By subtituting K_R=1, V_{DD}=5V, $V_{T(n)}$=0.8V, $V_{T(p)}$=-0.8V, they were obtained V_{IH}=2.925V, V_{IL}=2.075, V_{OH}=4.575V, and V_{OL}=0.425V. The calculated noise margin is 1.65 volts. Illustration of noise margin value calculated by formula in this research as shown in Figure 2.

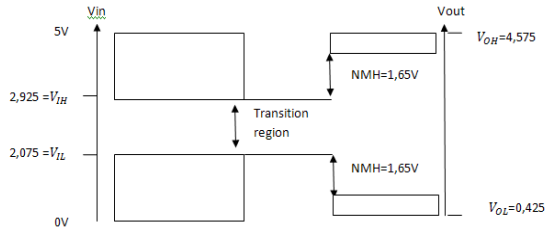

Figure 2. Noise Margin of Multiplexer 16 to 1

2.4 Propagation Delay

Time propagation delay (t_{PD}) consist of t_{PLH} and t_{PHL} can be affected by capacitor value occurs inside of the transistor circuit design. This study used propagation delay data from another datasheets as a comparison of speed. It shown that DM74150 CMOS IC has t_{PD}=34 ns and C=50 pF, on the other side MM150J TTL IC has t_{PD}= 220ns and C=50pF. In this design, by modification of internal capacitor HCMOS Multiplexer should be created with t_{PD} smaller than other ICs, and it has t_{PLH} and t_{PHL} 20ns approximately. This desired value smaller than the time propagation delay of TTL and CMOS ICs. Modification of the capacitance was done by adjusting trans-conductance to obtain suitable capacitance values and time propagation delay minimum. Table 3 shows the calculated parameter t_{PD} by modification of K_N/K_P and different internal capacitances.

Table 3. Calculated Data for Propagation Delay

K_N / K_P	Parameter (ns)	C_L (pF)					
		0,5	1	5	10	15	50
K_N = 5 µA/V² K_P = 2 µA/V²	t_{PLH}	16	32	160	320	480	1600
	t_{PHL}	16	32	160	320	480	1600
K_N = 10 µA/V² K_P = 4 µA/V²	t_{PLH}	8	16	80	160	240	800
	t_{PHL}	8	16	80	160	240	800
K_N = 15 µA/V² K_P = 6 µA/V²	t_{PLH}	5,33	10,67	53,35	106,66	160	533,33
	t_{PHL}	5,33	10,67	53,35	106,66	160	533,33
K_N = 20 µA/V² K_P = 8 µA/V²	t_{PLH}	4	8	40	80	120	400
	t_{PHL}	4	8	40	80	120	400
K_N = 25 µA/V² K_P = 10 µA/V²	t_{PLH}	3,2	6,4	32	64	96	320
	t_{PHL}	3,2	6,4	32	64	96	320
K_N = 30 µA/V² K_P = 12 µA/V²	t_{PLH}	2,66	5,33	26,65	53,33	80	266,66
	t_{PHL}	2,66	5,33	26,65	53,33	80	266,66
K_N = 35 µA/V² K_P = 14 µA/V²	t_{PLH}	2,29	4,57	22,85	45,71	68,57	228,57
	t_{PHL}	2,29	4,57	22,85	45,71	68,57	228,57
K_N = 40 µA/V² K_P = 16 µA/V²	t_{PLH}	2	4	20	40	60	200
	t_{PHL}	2	4	20	40	60	200

2.5 Power Dissipation

Power Dissipation (PD) is obtained by determining the operating frequency according to the capacitor used. One of parameters are used to indicate the speed of signal transitional response and the power consumsion of a gate is the minimum Power Delay Product (PDP). Power dissipation compared by datasheet value with varying of frequency and capacitor value at K_N=40 µA/V² and K_P=16 µA/V² A. This method evaluated power dissipation at 1, 4, 10, 20, and 25 MHz of signal input and various capacitors were calculated by previous method.

3. RESULT

3.1 Simulation of VTC

Voltage transfer characteristic of IC is shown in Figure 3(a). Based on the Figure 3(a), it can be determined value of V_{IH}, V_{IL}, V_{OH}, and V_{OL}. Ideal condition occurs when the V_{IL} close to ground (0V), while V_{OH} close to V_{DD} (5 V) and the difference between V_{IL} and V_{IH} is too small. The graph show value are V_{OH}= 5V, V_{IH}= 2.94V, V_{OL}= 0V, V_{IL} =2.92V. the noise margin calculated from simulation data is 2.92 volts.

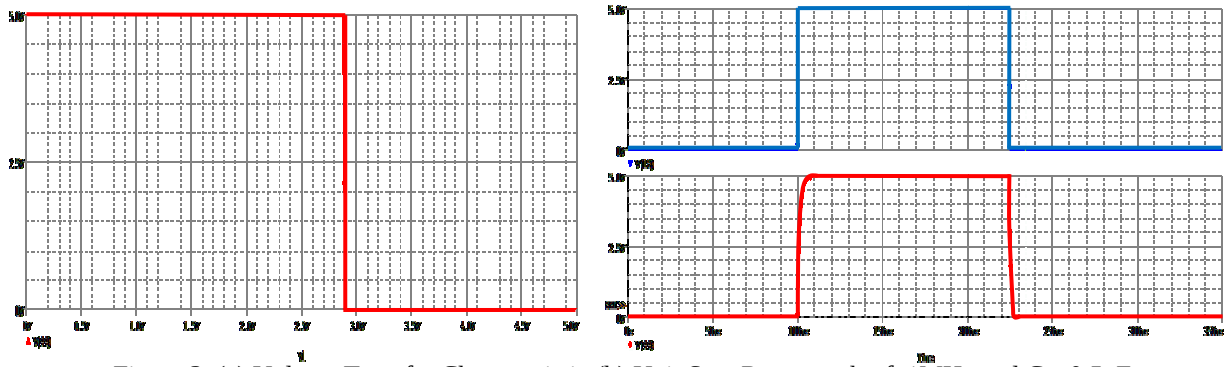

Figure 3. (a) Voltage Transfer Characteristic (b) Unit Step Response by *f*=1MHz and C_L=0.5pF

3.2 Simulation Result by Unit Step

Figure 3 (b) show the simulation result of unit step response by C_L = 0,5pF and 1MHz frequency. The Propagation delay, rise time, and falling time were obtained t_{PLH} =1.028 ns, t_{PHL} = 0.396ns, t_r = 3.13 ns, and t_f = 1,25 ns. Based on those data, time propagation delay (t_{PD}), PD and PDP are 0.7ns, 0.0125 mW and 8.75 fJ, respectively.

3.3 Comparison of the Simulation Results

Table 4 shows the comparison of the simulation result of 16 to 1 HCMOS Multiplexer IC with calculation method and other ICs. Simulation and the calculation results of the VTC value and Noise Margin does not have a significant difference and a small percentage of error obtained by Noise Margin in the simulation.

Table 4. Comparison result between simulation and other method

Parameters	Datasheet		calculation	simulation	%Error
	DM74150 Vcc = 5V	MM54C150 Vcc = 5V			
V_{IH} (V)	2	3,5	2,925	2,94	0,015
V_{IL} (V)	0,8	1,5	2,075	2,92	0,845
V_{OH} (V)	2,4	4,5	4,575	5	0,425
V_{OL} (V)	0,4	0,5	0,425	0	0,425
N_{MH}(V)	0,4	1	1,65	2,06	0,41
N_{ML}(V)	0,4	1	1,65	2,92	1,27

4. CONCLUSION

According to the analysis of the schematic and simulation result, this study could be concluded that:

- The 16 to 1 HCMOS Multiplexer IC consist of 5 inverter gates including 10 of PMOS and NMOS transistors, 16 NAND gate by 5 input consist of 160 PMOS and NMOS transistors, 1 NAND gate consist of 16 input consisting 32 PMOS and NMOS transistors and 1 cascade inverter including 4 PMOS and NMOS transistors. The number of CMOS transistors required to design the 16 to 1 HCMOS Multiplexer IC are 206 MOS transistors that each totaled 103 for PMOS and NMOS transistors.
- The design of the 16 to 1 HCMOS Multiplexer IC has Voltage Transfer characteristic (VTC) symmetrical with high logic of *noise margin* (N_{MH}) and low logic of *noise margin* (N_{ML}) each about 1,65V defined by V_{IL} = 2.075 V, V_{IH} = 2.925 V, V_{OL} = 0.425 V, and V_{OH} = 4.575 V, using simulation Result by *PSpice* obtained the value of VTCs are V_{IL} = 2.92 V, V_{IH} = 2.94 V, V_{OL} = 0 V, and V_{OH} = 5 V so the N_{MH} = 2.06 and N_{ML} = 2.92 V.
- This Multiplexer is designed with the *propagation delay* 20ns at C_L = 5 pF and power dissipation of 0,125 mW. Simulation of the Multiplexer 16 to 1 HCMOS by *PSpice* with C_L = 5 pF be obtained the *propagation delay* is better than calculation result of 9.79 ns.
- Simulation of the Multiplexer 16 to 1 HCMOS compared with the same capacitance (C_L = 15 pF for TTL and C_L = 50 pF for CMOS) obtain *propagation delay* value and power dissipation better than DM74150 TTL IC and MM54C150N CMOS IC. The HCMOS Multiplexer IC has area 610 µm x 210 µm of layout I/O pad and 1625.5 µm x 1625.5 µm with I/O pad.

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